REV: 101224

XMC-16AO16C

16-Channel 16-Bit High-Speed Analog Output Board

With 450,000 Samples per Second per Channel

Features Include:

- **16 Precision 16-Bit High-Speed Analog Output Channels; D/A Converter per Channel**
- **Balanced 3-Wire Differential Outputs, or Optional 2-Wire Single-ended Outputs with Remote Ground Sensing**
- **Data Rates to 450K Samples per Second per Channel; 7.2 MSPS Aggregate Rate**
- **Software-Selectable Output Ranges of ±10V, ±5V, ±2.5V or ±1.25V; Optional ±20V, ±10V, ±5V differential output ranges**
- **256K-Sample Output Data FIFO Buffer; Configurable as Open or Circular**
- **Two DMA channels available for buffer access in either Block-Mode or Demand-Mode**
- Simultaneous or Sequential Output Clocking
- Multiboard Synchronization Supported
- Continuous and Burst (One-Shot) Output Modes Support Seamless Waveform Sequencing
- Data Rate Controlled Internally or Externally
- Software-Selectable Differential Clock I/O for Synchronizing Sigma-Delta A/D Boards
- High Accuracy Ensured by On-Demand Autocalibration of all Channels
- Extended-temperature version available
- Available in PCIe Form Factor

Applications Include:

- ✓ Precision Voltage Source
- ✓ Audio Synthesis
- ✓ Acoustic Research
- ✓ Process Control
- ✓ Waveform Synthesis
- ✓ Industrial Robotics

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Overview:

The XMC-16AO16C board contains sixteen 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed differential or single-ended analog output capability to a XMC application. Output ranges are software-selectable as ±10 Volts, ±5 Volts or ±2.5 Volts. The board is functionally compatible with the IEEE PCI Express bus specification Revision 1.0a. Unique FIFO buffer controls support the seamless sequencing of successive waveforms through a single buffer port. In less demanding applications, the outputs can be updated individually. Hardware clock I/O permits synchronization with a variety of GSC products, including Sigma-Delta ADC boards.

A PCIe interface adapter provides the interface between the controlling PCIe bus and the internal local controller (Figure 1). Sixteen output channels are controlled through an analog output FIFO buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including autocalibration. Analog output levels are initialized to zero (midrange). Multiboard synchronization is supported.

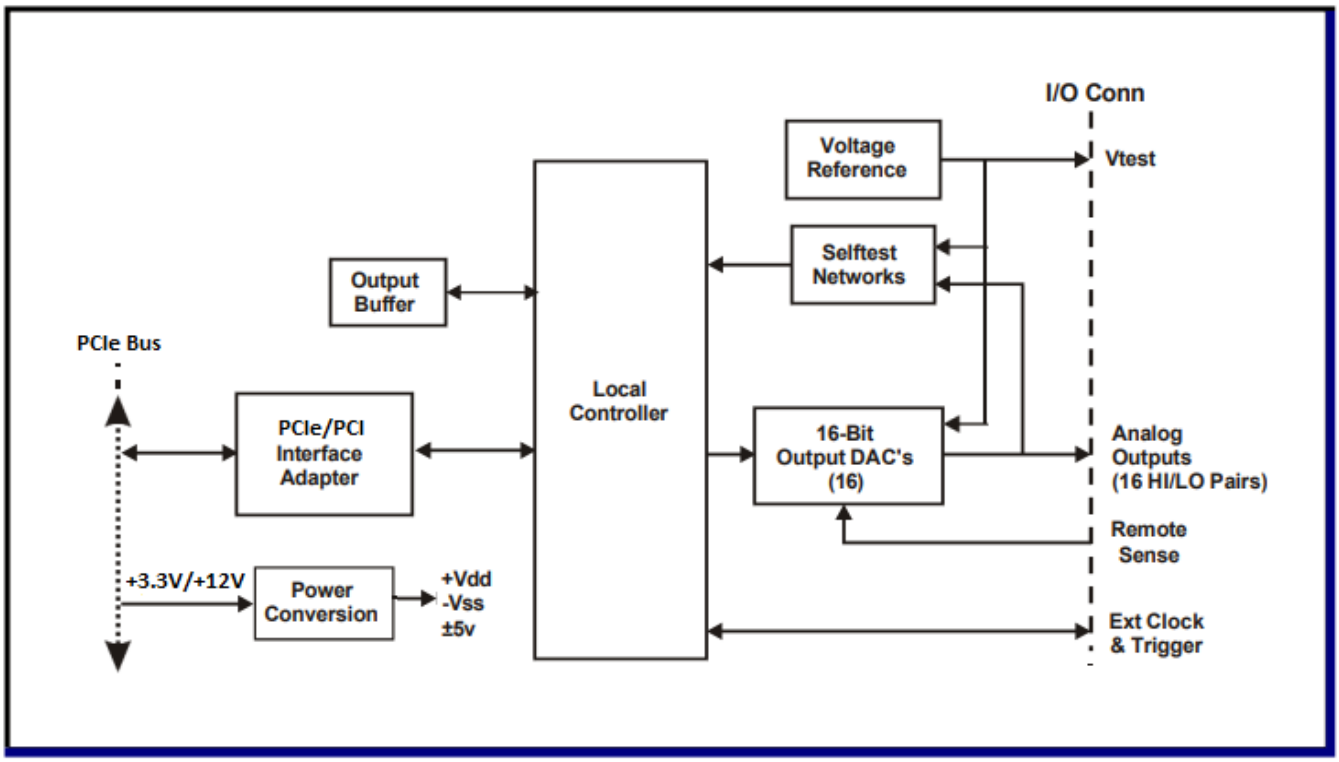


Figure 1. XMC-16AO16C Board; Functional Organization

This product is designed for minimum off-line maintenance. On-demand autocalibration eliminates the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 68-pin I/O connector. Power requirements consist of +3.3 VDC and +12V, in compliance with the PCIe specification, and operation over the specified temperature range is achieved with conventional convection cooling.

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Electrical Specifications

(At +25 ^{O}C, with specified operating conditions)

Analog Output Channels

Output Characteristics:

Configuration:	Sixteen 3-wire balanced differential analog output channels, with a dedicated 16-Bit DAC per channel. Each 3-Wire output consists of complementary 'HI' and 'LO' signal lines, with 'output return' as the center (balance) reference. All output returns are electrically common internally. Optional 12-channel and 8-Channel configurations are available, as well as 2-wire single-ended analog outputs with remote ground sensing.
Voltage Ranges:	Software-selected as ±10V, ±5V, ±2.5Vor ±1.25V, Line-to-Line for differential configuration. Line-to-Ground with Single-Ended option (Output-HI relative to output return). Optional High-Level (HL) ±20V, ±10V, ±5V differential outputs. See Ordering information.
Output Resistance:	1.0 Ohm maximum
Protection:	Withstands sustained short-circuiting to ground without damage
Load Current:	±3 ma maximum on all channels simultaneously; ±2 ma recommended for minimal crosstalk and line loss. (10mA maximum on individual channels, if total load on all outputs does not exceed 50mA).
Load Capacitance:	Stable with zero to 10,000 pF shunt capacitance; all ranges, all loads.
Settling Time (Typical):	No Filter: 5 us to 0.1%, 8 us to 0.01% 100 kHz Filter: 14 us to 0.1%, 18 us to 0.01% 10 kHz Filter: 100 us to 0.1%, 140 us to 0.01%
Noise:	No Filter: 1.3 mVRMS, 10Hz-10MHz 10 kHz Filter: 0.4 mVRMS, 10Hz-10MHz
Glitch Impulse:	±2.5V Range: 3 nV-Sec max. ±10V Range: 8 nV-Sec
Remote Sensing: (Single-ended outputs)	Single input pin compensates for ground potential at load. Max range ±1.0V. Enabled or disabled through application software. Correction ±1 percent. Input resistance: 15K typical.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Clocking Rate:	Internal Rate Clock: 172 to 450,000 samples per second per channel External Rate Clock: 0 to 450,000 samples per second per channel

DC Accuracy, Line-Line: (Max error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±20V	±6.2mv	±15mv
±10V	±2.4mv	±3.3mv
±5V	±1.7mv	±2.2mv
±2.5V	±1.4mv	±1.6mv
±1.25V	±1.2mv	±1.4mv

Output Balance:	10mV maximum HI/LO unbalance.
Bandwidth	10 kHz, 100 kHz and No-Filter (>300 kHz) options, Typical at -3dB. (Single-pole lowpass)
Crosstalk Rejection:	80 dB minimum, DC-50 kHz
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Operating Modes and Control

DAC Clocking Source:	Internal rate generator, external hardware input, or software clock. The internal rate generator is selectable as either (a) a division of the 45MHz master clock oscillator, or (b) a software-controlled VCO with 0.2% setting resolution, and ±0.02% accuracy.
Multiboard Clocking Configurations:	To support the simultaneous clocking of DAC outputs on multiple boards, the 16AO16 can be software-designated as either a clock initiator or a clock target. Initiators provide an output clock for target boards, each of which can retransmit the clock signal to subsequent boards connected in a daisy-chain configuration.
Burst Trigger:	Software control bit, or external TTL/LVDS trigger input (Same as clock I/O option). Burst triggering also can be obtained from an external source.
Update Mode:	Simultaneous or channel-sequential output updating
Active Buffer Size:	From 8 output values to 256K-values, in 2:1 steps, software-selectable.
Buffer Mode:	Selected as Circular for periodic waveforms, or as Open for one-shot functions
Data Format:	Software selected as Offset Binary or Two's complement

PCIe Compatibility

Conforms to PCI Express Specification revision 1.0a; x1 Link operating at 2.5Gbps. DMA transfers as bus master with two DMA channels.

Supports both block-mode and demand-mode DMA transfers as bus master.

Power, Mechanical and Environmental Specifications

Power Requirements:

+3.3VDC ±0.2 VDC, 0.4 Amps typical, 0.5 Amp maximum.
+12VDC ±0.4 VDC, 0.5 Amps typical, 0.7 Amps maximum
Total power consumption: 6 Watts typical, 10 Watts maximum.

Mechanical Characteristics:

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

Power, Mechanical and Environmental Specifications (Continued)

Environmental Requirements:

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +85 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

Ordering Information

Specify the basic model number, followed by an option suffix "-A-B-C-D", as indicated below. For example, model number XMC-16AO16C-16-F10-DF describes a XMC module with 16 output channels, 10 kHz output filters, with the outputs configured for differential.
(The "-D" option field may be left blank if not used).

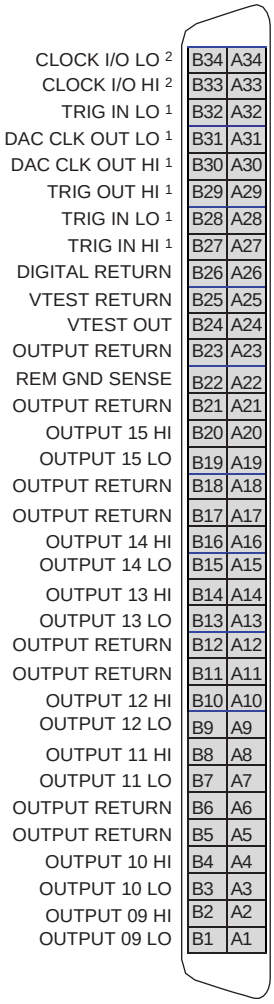
Optional Parameter	Value	Specify Option As:
Number of Output Channels:	**8 Channels**	**A = 8**
	12 Channels	**A= 12**
	16 Channels	**A = 16**
Output Lowpass Filter: (Single-pole)	**No output Filters (>300kHz)**	**B = F0**
	10 kHz Output Filters	**B = F10**
	100 kHz Output Filters	**B = F100**
Output Configuration:*	**Differential**	**C = DF**
	Single-Ended	**C = SE**
Custom Feature:	**High-Level Differential Outputs (±20V,±10V, ±5V differential output ranges)**	**D = HL**
	49.152MHz Clock Oscillator	**D = 49.152M**
	44.982MHz Clock Oscillator	**D = 44.982M**
	(TBD)	**---**

* Differential outputs are essentially immune to ground potential differences, and do not implement compensation for ground potential at the load. Single-ended outputs are affected by remote ground potentials however, and are supported with a Remote Ground Sense input to compensate for potential differences between the XMC-16AO16C outputs and the load.

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

I/O Connector Pin Assignment

(AMP 787170-7, 68 Position D-Type Receptacle)
(*Original pin list shown below*)



CLOCK I/O LO [2]	B34	A34	OUTPUT 08 HI
CLOCK I/O HI [2]	B33	A33	OUTPUT 08 LO
TRIG IN LO [1]	B32	A32	OUTPUT RETURN
DAC CLK OUT LO [1]	B31	A31	OUTPUT RETURN
DAC CLK OUT HI [1]	B30	A30	OUTPUT 07 HI
TRIG OUT HI [1]	B29	A29	OUTPUT 07 LO
TRIG IN LO [1]	B28	A28	OUTPUT RETURN
TRIG IN HI [1]	B27	A27	OUTPUT RETURN
DIGITAL RETURN	B26	A26	OUTPUT 06 HI
VTEST RETURN	B25	A25	OUTPUT 06 LO
VTEST OUT	B24	A24	OUTPUT RETURN
OUTPUT RETURN	B23	A23	OUTPUT RETURN
REM GND SENSE	B22	A22	OUTPUT 05 HI
OUTPUT RETURN	B21	A21	OUTPUT 05 LO
OUTPUT 15 HI	B20	A20	OUTPUT RETURN
OUTPUT 15 LO	B19	A19	OUTPUT RETURN
OUTPUT RETURN	B18	A18	OUTPUT 04 HI
OUTPUT RETURN	B17	A17	OUTPUT 04 LO
OUTPUT 14 HI	B16	A16	OUTPUT RETURN
OUTPUT 14 LO	B15	A15	OUTPUT RETURN
OUTPUT 13 HI	B14	A14	OUTPUT 03 HI
OUTPUT 13 LO	B13	A13	OUTPUT 03 LO
OUTPUT RETURN	B12	A12	OUTPUT RETURN
OUTPUT RETURN	B11	A11	OUTPUT RETURN
OUTPUT 12 HI	B10	A10	OUTPUT 02 HI
OUTPUT 12 LO	B9	A9	OUTPUT 02 LO
OUTPUT 11 HI	B8	A8	OUTPUT RETURN
OUTPUT 11 LO	B7	A7	OUTPUT RETURN
OUTPUT RETURN	B6	A6	OUTPUT 01 HI
OUTPUT RETURN	B5	A5	OUTPUT 01 LO
OUTPUT 10 HI	B4	A4	OUTPUT RETURN
OUTPUT 10 LO	B3	A3	OUTPUT RETURN
OUTPUT 09 HI	B2	A2	OUTPUT 00 HI
OUTPUT 09 LO	B1	A1	OUTPUT 00 LO

The differential analog output configuration is shown.
For optional single-ended outputs, OUTPUT XX HI is an output, and OUTPUT XX LO should be left disconnected.

[1] Software-selectable as LVDS differential pairs. In TTL mode, 'HI' pins are signal pins, and 'LO' inputs should be connected to digital return.
[2] Bidirectional synchronization signal.

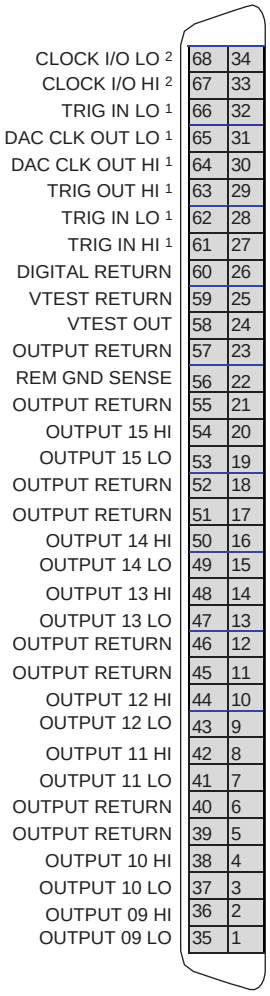
System Cable Mating Connector:

68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com

I/O Connector Pin Assignment

(AMP 787170-7, 68 Position D-Type Receptacle)



CLOCK I/O LO [2]	68	34	OUTPUT 08 HI
CLOCK I/O HI [2]	67	33	OUTPUT 08 LO
TRIG IN LO [1]	66	32	OUTPUT RETURN
DAC CLK OUT LO [1]	65	31	OUTPUT RETURN
DAC CLK OUT HI [1]	64	30	OUTPUT 07 HI
TRIG OUT HI [1]	63	29	OUTPUT 07 LO
TRIG IN LO [1]	62	28	OUTPUT RETURN
TRIG IN HI [1]	61	27	OUTPUT RETURN
DIGITAL RETURN	60	26	OUTPUT 06 HI
VTEST RETURN	59	25	OUTPUT 06 LO
VTEST OUT	58	24	OUTPUT RETURN
OUTPUT RETURN	57	23	OUTPUT RETURN
REM GND SENSE	56	22	OUTPUT 05 HI
OUTPUT RETURN	55	21	OUTPUT 05 LO
OUTPUT 15 HI	54	20	OUTPUT RETURN
OUTPUT 15 LO	53	19	OUTPUT RETURN
OUTPUT RETURN	52	18	OUTPUT 04 HI
OUTPUT RETURN	51	17	OUTPUT 04 LO
OUTPUT 14 HI	50	16	OUTPUT RETURN
OUTPUT 14 LO	49	15	OUTPUT RETURN
OUTPUT 13 HI	48	14	OUTPUT 03 HI
OUTPUT 13 LO	47	13	OUTPUT 03 LO
OUTPUT RETURN	46	12	OUTPUT RETURN
OUTPUT RETURN	45	11	OUTPUT RETURN
OUTPUT 12 HI	44	10	OUTPUT 02 HI
OUTPUT 12 LO	43	9	OUTPUT 02 LO
OUTPUT 11 HI	42	8	OUTPUT RETURN
OUTPUT 11 LO	41	7	OUTPUT RETURN
OUTPUT RETURN	40	6	OUTPUT 01 HI
OUTPUT RETURN	39	5	OUTPUT 01 LO
OUTPUT 10 HI	38	4	OUTPUT RETURN
OUTPUT 10 LO	37	3	OUTPUT RETURN
OUTPUT 09 HI	36	2	OUTPUT 00 HI
OUTPUT 09 LO	35	1	OUTPUT 00 LO

The differential analog output configuration is shown.
For optional single-ended outputs, OUTPUT XX HI is an output, and OUTPUT XX LO should be left disconnected.

[1] Software-selectable as LVDS differential pairs. In TTL mode, 'HI' pins are signal pins, and 'LO' inputs should be connected to digital return.
[2] Bidirectional synchronization signal.

System Cable Mating Connector:

68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com