PCIe4-SIO8BX2V-FASYNC

Hardware User's Manual

FAST ASYNC SERIAL I/O PCIe CARD

FEATURING RS422/RS485 TRANSCEIVERS
AND 32K BYTE FIFO BUFFERS (512K BYTE TOTAL)

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PREFACE

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EIA-422-A – Electrical Characteristics of Balanced Voltage Digital Interface Circuits
(EIA order number EIA-RS-422A)

EIA-485 – Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems
(EIA order number EIA-RS-485)

EIA Standards and Publications can be purchased from:

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PCI Local Bus Specification Revision 2.2 December 18, 1998

Copies of PCI specifications available from:
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CHAPTER 1: INTRODUCTION

1.0 General Description

The PCIe4-SIO8BX2V-FASYNC provides for 8 channels of fast asynchronous serial operation. The asynchronous interface is a standard async interface. 8x oversampling is used based on the programmable clock. Each channel may be set to a different baud rate. The programmable clock may be set up to 80MHz, which provides up to a baud rate up to 10Mbps.

The PCIe4-SIO8BX2V-FASYNC board is based on the SIO4BX product line from General Standards Corporation. In order to maintain software compatibility, the PCIe4-SIO8BX2V is implemented as two independent four channel SIO4BX2 cards. This manual applies to each of the 4 channel cards.

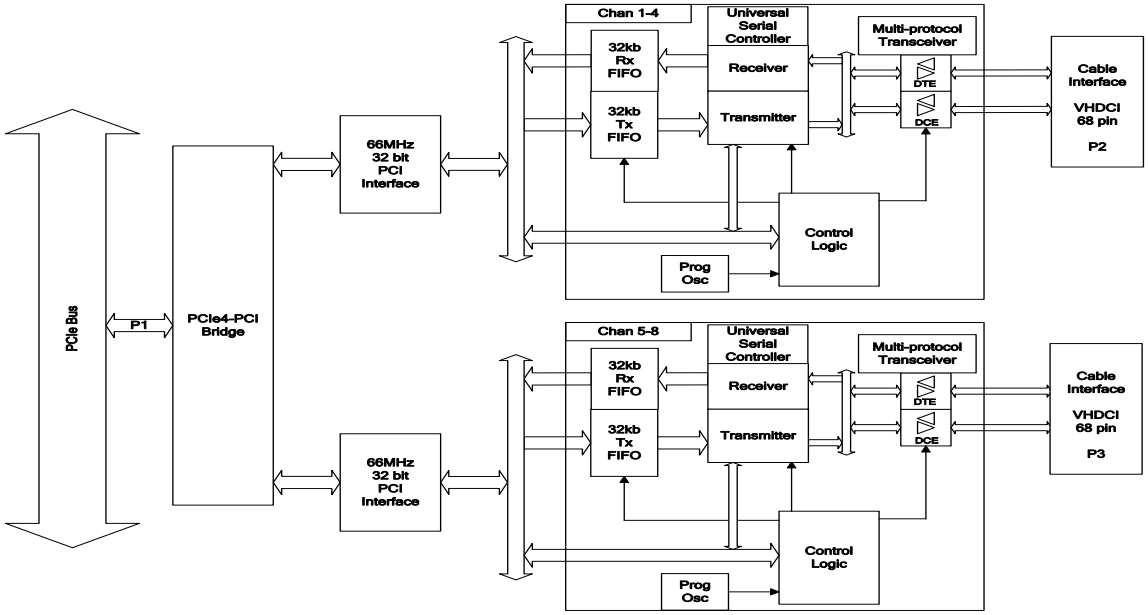


Figure 1-1 Block Diagram of PCIe4-SIO8BX2V

- Four Lane PCI Express (PCIe4) Interface
- Four Independent RS422/RS485 Serial Channels
- Fast RS422/RS485 Differential Cable Transceivers Provide Data Rates up to 10Mbps
- Programmable Oscillators provide increased flexibility for Baud Rate Clock generation
- Eight signals per channel, configurable as either DTE or DCE:
  2 Serial Data (TxD, RxD), 2 Flow Control (RTS, CTS), plus 4 General Purpose
- Independent Transmit and Receive FIFOs for each Serial Channel – 32K byte each
- Programmable Transmit Gap Bit Counts allow for variable gap between words
- Standard Cables - VHDCI to four DB25 connectors (2 per board). Custom Cables available
- Standard Cable to four DB25 connectors and Custom Cables available
- Available drivers include Win10 and Linux (Inquire for Others)
- Industrial Temperature Option Available

1.1 Serial Interface

The simple fast asynchronous interface consists of two Data signals (TxD /RxD) and two optional Control signals (RTS / CTS). The Fast Async serial protocol can be customized with the following user configurable options:

- Channel Speed 10Mbps down to 50bps on a per channel basis.
- Parity: Selectable Even / Odd/ Mark/ Space/ No Parity
- Stop Bits: 1 or 2
- Transmit Gap Size: 0 to 64k bits.
  (Transmit Gap Size is the number of extra stop bits between transmit words)

The Data Word length is set at 8 Bits and is transmitted LSB first. The signal encoding is NRZ.

1.2 Deep Transmit/Receive FIFOs

Data is transferred to/from the serial interface through Transmit and Receive FIFOs. Each of the four serial channels has an independent Transmit FIFO and a Receive FIFO for a total of eight separate on-board FIFOs. These FIFOs are always 32K bytes deep. FIFOs allow data transfer to continue to/from the IO interface independent of PCI interface transfers and software overhead.

The SIO8BX2V provides access to complete FIFO status to optimize data transfers. In addition to Empty and Full indicators, each FIFO has a programmable Almost Empty Flag and a programmable Almost Full Flag. These FIFO flags may be used as interrupt sources to monitor FIFO fill levels. In addition, real-time FIFO counters showing the exact number of words in the FIFO are also provided for each FIFO. By utilizing these FIFO counters, data transfers can be optimized to efficiently send and receive data.

1.3 Transceiver Protocol

Since the SIO8BX2V-FASYNC is a fast interface, high-speed RS422/RS485 transceivers are implemented. For slower RS232 serial interface, please use the Standard PCIE4-SIO8BX2V variation. Each channel direction may also be configured as DTE or DCE configuration. This allows for either full duplex or half duplex configurations.

1.4 General Purpose IO

There are sixteen General Purpose IO signals available (4 per channel). These can be used as inputs, or hi/lo outputs under software control. These are controlled with the Channel Pin Source and Channel Pin Status registers.

1.5 Connector Interface

The SIO8BX2V provides a user IO interface through two front-side card edge connectors. Four serial channels interface through each high-density, 68 pin VHDCI type connector, and are grouped to simplify separating the cable into four distinct serial connectors.

Standard cables are available from General Standards in various lengths to adapt the single 68 pin VHDCI connector into four DB25 connectors (one per channel). A standard cable is also available with a single 68 pin VHDCI connector on one end and open on the other. This allows the user to add a custom connector (or connect to a terminal block). General Standards will also work with customers to fabricate custom cables. Consult factory for details on custom cables.

CHAPTER 2: LOCAL SPACE REGISTERS

2.0 GSC Firmware (Local Space) Registers Description

The PCIe4-SIO8BX2V-FASYNC is accessed through two sets of registers – PCI Registers and GSC Firmware Registers. The GSC Firmware Registers (also referred to as Local Space Registers), which provide the control/status for the board, are described below. The PCI registers (internal to the PLX 9056 PCI controller) are discussed in Chapter 4.

Offset Address	Access*	Register Name	Default Value (Hex)
0x0000	Read Only	Firmware Revision	E50808XX
0x0004	Read/Write	Board Control	00000000
0x0008	Read Only	Board Status	000000XX
0x000C	Read Only	RESERVED	00000000
0x0010	Read/Write	Ch 1 Tx Almost Full/Empty	00070007
0x0014	Read/Write	Ch 1 Rx Almost Full/Empty	00070007
0x0018	Read/Write	Ch l Data FIFO	000000XX
0x001C	Read/Write	Ch 1 Control/Status	0000CC00
0x0020	Read/Write	Ch 2 Tx Almost Full/Empty	00070007
0x0024	Read/Write	Ch 2 Rx Almost Full/Empty	00070007
0x0028	Read/Write	Ch 2 Data FIFO	000000XX
0x002C	Read/Write	Ch 2 Control/Status	0000CC00
0x0030	Read/Write	Ch 3 Tx Almost Full/Empty	00070007
0x0034	Read/Write	Ch 3 Rx Almost Full/Empty	00070007
0x0038	Read/Write	Ch 3 Data FIFO	000000XX
0x003C	Read/Write	Ch 3 Control/Status	0000CC00
0x0040	Read/Write	Ch 4 Tx Almost Full/Empty	00070007
0x0044	Read/Write	Ch 4 Rx Almost Full/Empty	00070007
0x0048	Read/Write	Ch 4 Data FIFO	000000XX
0x004C	Read/Write	Ch 4 Control/Status	0000CC00
0x0050-0x005C	--	RESERVED	--------
0x0060	Read/Write	Interrupt Control	00000000
0x0064	Read/Write	Interrupt Status/Clear	00000000
0x0068	Read Only	Interrupt Edge/Level	FFFFFFFF
0x006C	Read/Write	Interrupt High/Low	FFFFFFFF
0x0070	Read/Write	Ch 1 Async Control/Status	00000000
0x0074	Read/Write	Ch 2 Async Control/Status	00000000
0x0078	Read/Write	Ch 3 Async Control/Status	00000000
0x007C	Read/Write	Ch 4 Async Control/Status	00000000
0x0080	Read/Write	Ch 1Pin Source	00000000
0x0084	Read/Write	Ch 2 Pin Source	00000000
0x0088	Read/Write	Ch 3 Pin Source	00000000
0x008C	Read/Write	Ch 4 Pin Source	00000000
0x0090	Read Only	Ch 1Pin Status	000000XX
0x0094	Read Only	Ch 2 Pin Status	000000XX
0x0098	Read Only	Ch 3 Pin Status	000000XX
0x009C	Read Only	Ch 4 Pin Status	000000XX
0x00A0	Read/Write	Prog Osc RAM Addr	00000000
0x00A4	Read/Write	Prog Osc RAM Data (Ch 1-3)	XXXXXXXX
0x00A8	Read/Write	Prog Osc Control/Status	00000000
0x00AC	Read/Write	Prog Osc RAM Data (Ch 4)	XXXXXXXX

0x00B0	Read/Write	Ch1 Tx Gap	00000000
0x00B4	Read/Write	Ch2 Tx Gap	00000000
0x00B8	Read/Write	Ch3 Tx Gap	00000000
0x00BC	Read/Write	Ch4 Tx Gap	00000000
0x00C0-0x00CC	--	RESERVED	--------
0x00D0	Read Only	Ch1 FIFO Count	00000000
0x00D4	Read Only	Ch2 FIFO Count	00000000
0x00D8	Read Only	Ch3 FIFO Count	00000000
0x00DC	Read Only	Ch4 FIFO Count	00000000
0x00E0	Read Only	Ch1 FIFO Size	XXXXXXXX
0x00E4	Read Only	Ch2 FIFO Size	XXXXXXXX
0x00E8	Read Only	Ch3 FIFO Size	XXXXXXXX
0x00EC	Read Only	Ch4 FIFO Size	XXXXXXXX
0x00F0-0x00F4	--	RESERVED	--------
0x00F8	Read/Write	FW Type Register	08080808
0x00FC	Read Only	Features Register	00613AF4

2.1 Firmware Revision: Local Offset 0x0000

The Firmware Revision Register provides version information about the firmware on the board. This is useful for technical support to identify the firmware version.

D31:16	HW Board Rev	0xE508	PCIe4-SIO8BX2V Rev F
D15:8	Firmware Type ID	0x08	FAsync Firmware
D7:0	Firmware Revision	XX	Firmware Version

2.2 Board Control: Local Offset 0x0004

The Board Control Register defines the general control functions for the board. The main function in this register defines the Demand mode DMA channel requests.

D31 Board Reset
1 = Reset all Local Registers and FIFOs to their default values
Notes: This bit will automatically clear to 0 following the board reset.
Board Reset will NOT reset programmable oscillator.

D30:27 RESERVED

D26 LED D2
1 = Turn on green LED D2

D25 LED D3
1 = Turn on green LED D3

D24 LED D4
1 = Turn on green LED D4

D23:D8 RESERVED

D7	Demand Mode DMA Channel 1 Single Cycle Disable
D6:4	Demand Mode DMA Channel 1 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx
D3	Demand Mode DMA Channel 0 Single Cycle Disable
D2:0	Demand Mode DMA Channel 0 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx

2.3 Board Status: Local Offset 0x0008

The Board Status Register gives general overall status for a board. The Board Jumpers (D3:D0) are physical jumpers which can be used to distinguish between boards if multiple SIO4 boards are present in a system.

D31:D4	RESERVED
D3:D0	Board Jumper (J5)
D3	Board ID4 1=J5:7-J5:8 jumper installed
D2	Board ID3 0=J5:5-J5:6 jumper installed
D1	Board ID2 0=J5:3-J5:4 jumper installed
D0	Board ID1 0=J5:1-J5:2 jumper installed

2.4 Channel TX Almost Flags: Local Offset 0x0010 / 0x0020 / 0x0030 / 0x0040

The Tx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the transmit FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16 TX Almost Full Flag Value
Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains {FIFO Size – Almost Full Value} words or more.)

D15:0 TX Almost Empty Flag Value
Number of words from FIFO Empty when the Almost Empty Flag will be asserted.

2.5 Channel Rx Almost Flags: Local Offset 0x0014 / 0x0024 / 0x0034 / 0x0044

The Rx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the receive FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16 RX Almost Full Flag Value
Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains {FIFO Size – Almost Full Value} words or more.)

D15:0 RX Almost Empty Flag Value
Number of words from FIFO Empty when the Almost Empty Flag will be asserted

2.6 Channel FIFO: Local Offset 0x0018 / 0x0028 / 0x0038 / 0x0048

The Channel FIFO Register passes serial data to/from the serial controller. The same register is used to access both the Transmit FIFO (writes) and Receive FIFO (reads).

D31:8 RESERVED
D7:0 Channel FIFO Data

2.7 Channel Control/Status: Local Offset 0x001C / 0x002C / 0x003C / 0x004C

The Channel Control/Status Register provides the reset functions and data transceiver enable controls, and the FIFO Flag status for each channel.

D31:19 Channel Control Bits

D31:28 RESERVED

D26 Stop Transmit On FIFO Empty
0 = Transmitter remains enabled under software control (D25)
1 = Transmitter will be disabled (D25 = '0') if Tx FIFO becomes empty

D25 Transmit Enable
1 = Transmitter enabled.
Note: Transceiver must be Enabled and DTE/DCE Direction set before Transmitter Enabled.

D24 Receive Enable
1 = Receiver enabled.
Note: Transceiver must be Enabled and DTE/DCE Direction set before Receiver Enabled.

D23:20 LED Control
Each Channel controls 2 LEDs on the back of PCB.
Note: See Section 5.3 for more detailed information about the LED Control.

D19 Rx Stop on Full
0 = Receiver remains enabled under software control (D24)
1 = Receiver will be disabled (D24 = '0') if Rx FIFO becomes full

D18:8 Channel Status Bits

D18 Rx FIFO Underflow (Latched)
1= User Read Rx FIFO while empty (data invalid).
Note: This bit is latched. Write D18=1 to clear.

D17 Tx FIFO Overflow (Latched)
1= User Wrote Tx FIFO while full (data lost).
Note: This bit is latched. Write D17=1 to clear.

D16 Rx FIFO Overflow (Latched)
1= Rx Data was lost due to Rx Overflow.
Note: This bit is latched. Write D16=1 to clear.

D15	Rx FIFO Full Flag Lo	(0 = Rx FIFO Full)
D14	Rx FIFO Almost Full Flag Lo	(0 = Rx FIFO Almost Full)
D13	Rx FIFO Almost Empty Flag Lo	(0 = Rx FIFO Almost Empty)
D12	Rx FIFO Empty Flag Lo	(0 = Rx FIFO Empty)
D11	Tx FIFO Full Flag Lo	(0 = Tx FIFO Full)
D10	Tx FIFO Almost Full Flag Lo	(0 = Tx FIFO Almost Full)
D9	Tx FIFO Almost Empty Flag Lo	(0 = Tx FIFO Almost Empty)
D8	Tx FIFO Empty Flag Lo	(0 = Tx FIFO Empty)

D7:0 Channel Control Bits

D7 RESERVED

D6 Channel Reset (Pulsed)
Note: This value will automatically clear to '0'.

D5:D2 RESERVED

D1 Reset Channel Rx FIFO (Pulsed)
Note: This value will automatically clear to '0'.

D0 Reset Channel Tx FIFO (Pulsed)
Note: This value will automatically clear to '0'.

2.8 Interrupt Registers

There are 32 on-board interrupt sources (in addition to PLX interrupts), each of which may be individually enabled. Four interrupt registers control the on-board interrupts – Interrupt Control, Interrupt Status, Interrupt Edge/Level, and Interrupt Hi/Lo. The Interrupt sources are:

IRQ #	Source	Default Level	Alternate Level
IRQ0	Ch1 Parity Error	Rising Edge	Falling Edge
IRQ1	Ch1 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ2	Ch1 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ3	Ch1 Frame Error	Rising Edge	Falling Edge
IRQ4	Ch2 Parity Error	Rising Edge	Falling Edge
IRQ5	Ch2 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ6	Ch2 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ7	Ch2 Frame Error	Rising Edge	Falling Edge
IRQ8	Ch3 Parity Error	Rising Edge	Falling Edge
IRQ9	Ch3 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ10	Ch3 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ11	Ch3 Frame Error	Rising Edge	Falling Edge
IRQ12	Ch4 Parity Error	Rising Edge	Falling Edge
IRQ13	Ch4 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ14	Ch4 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ15	Ch4 Frame Error	Rising Edge	Falling Edge
IRQ16	Ch1 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ17	Ch1 Tx FIFO Full	Rising Edge	Falling Edge
IRQ18	Ch1 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ19	Ch1 Rx FIFO Full	Rising Edge	Falling Edge
IRQ20	Ch2 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ21	Ch2 Tx FIFO Full	Rising Edge	Falling Edge
IRQ22	Ch2 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ23	Ch2 Rx FIFO Full	Rising Edge	Falling Edge
IRQ24	Ch3 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ25	Ch3 Tx FIFO Full	Rising Edge	Falling Edge
IRQ26	Ch3 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ27	Ch3 Rx FIFO Full	Rising Edge	Falling Edge
IRQ28	Ch4 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ29	Ch4 Tx FIFO Full	Rising Edge	Falling Edge
IRQ30	Ch4 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ31	Ch4 Rx FIFO Full	Rising Edge	Falling Edge

For all interrupt registers, the IRQ source (IRQ31:IRQ0) will correspond to the respective data bit (D31:D0) of each register (D0 = IRQ0, D1 = IRQ1, etc.).

All FIFO interrupts are edge triggered active high. This means that an interrupt will be asserted (assuming it is enabled) when a FIFO Flag transitions from FALSE to TRUE (rising edge triggered) or TRUE to FALSE (falling edge). For example: If Tx FIFO Empty Interrupt is set for Rising Edge Triggered, the interrupt will occur when the FIFO transitions from NOT EMPTY to EMPTY. Likewise, if Tx FIFO Empty Interrupt is set as Falling Edge Triggered, the interrupt will occur when the FIFO transitions from EMPTY to NOT EMPTY.

All Interrupt Sources share a single interrupt request back to Local Interrupt Input of the PCI9056 PLX chip. This Local Interrupt input must be enabled in the PLX Interrupt Control/Status Register to be recognized as a PCI interrupt source.

2.8.1 Interrupt Control: Local Offset 0x0060

The Interrupt Control register individually enables each interrupt source. (1=Enabled / 0=Disabled). An interrupt source must be enabled for an interrupt to be generated.

2.8.2 Interrupt Status / Clear: Local Offset 0x0064

The Interrupt Status Register shows the status of each respective interrupt source. If an interrupt source is enabled in the Interrupt Control Register, a '1' indicates the respective interrupt has occurred. The interrupt source will remain latched until the interrupt is cleared, either by writing a '1' to the Interrupt Status/Clear Register in the respective interrupt bit position, or the interrupt is disabled in the Interrupt Control Register. Clearing an interrupt which is not enabled or not asserted will have no effect.

2.8.3 Interrupt Edge/Level: Local Offset 0x0068 (Read Only)

All interrupt sources are edge triggered.

2.8.4 Interrupt Hi/Lo: Local Offset 0x006C

The Interrupt Hi/Lo Register defines each interrupt source as rising edge or falling edge. For example, a rising edge of the TX Empty source will generate an interrupt when the TX FIFO becomes empty. Defining the source as falling edge will trigger an interrupt when the TX FIFO becomes "NOT Empty"

2.9 Async Control/Status: Local Offset 0x0070 / 0x0074 / 0x0078 / 0x007C

Async Status Bits – D31:D23 (Read Only)

D31 RESERVED
D30 TxGap-In-Progress
1 = Transmitter currently in TxGap delay
D29 CTS Input (Valid only when Transmitter Enabled)
D28 RxD Input (Valid only when Receiver Enabled)
D27 Transmitter Enabled
1 = Transmitter currently enabled
Note: If Transmit Enable (D25 in Channel Control) is disabled while Transmit-In-Progress, this bit will remain set until transmit is complete.
D26 Transmit-In-Progress
1 = Actively transmitting a byte
D25 Receiver Enabled
1 = Receiver currently enabled
Note: If Receiver Enable Bit D24 in Channel Control is disabled while Receive-In-Progress, this bit will remain set until receive is complete.
D24 Receive-In-Progress
1 = Actively receiving a byte

Async Controls Bits – D24:D0

D23:19 RESERVED

D18 Check Stop Bit 2 Frame Error
- 0 = Second Stop Bit invalid will not set Frame Error (if 2 Stop Bits)
- 1 = Second Stop Bit invalid will set Frame Error (if 2 Stop Bits)

D17 Save Data on Rx Frame Error
- 0 = Rx Data Byte will NOT be saved if a Frame Error is detected
- 1 = Rx Data Byte will be saved if a Frame Error is detected

D16 Save Data on Rx Parity Error
- 0 = Rx Data Byte will NOT be saved if a Parity Error is detected
- 1 = Rx Data Byte will be saved if a Parity Error is detected

D15:14 RESERVED

D13 CTS Function
- 0 = Input
- 1 = Auto Input – Transmit only if CTS Active

D12:10 RTS Source
- 00X =Disabled
- 010 = Output Lo (Inactive)
- 011 = Output Hi (Active)
- 100 = Auto Output – Output Hi if Rx Enabled
- 101 = Auto Output –Output Hi if Rx Not Almost Full
- 1XX = RESERVED

D9:8 TxD Source
- 00 = TxD Output
- 01 = RESERVED
- 10 = Output Lo (Inactive)
- 11 = Output Hi (Active)

D7:6 RESERVED

D5:4 Parity Type
- 00 = Even Parity
- 01 = Odd Parity
- 10 = Space Parity (Always 0)
- 11 = Mark Parity (Always 1)

D3 Parity Bit Enable
- 1 = Parity Bit Enabled

D2 Stop Bits
- 0 = 1 Stop Bit
- 1 = 2 Stop Bits

D1:0 RESERVED

2.10 Channel Pin Source: Local Offset 0x0080 / 0x0084 / 0x0088 / 0x008C

The Channel Pin Source Register configures the function of the cable interface signals as well as controls the transceiver protocols.

D31 Cable Transceiver Enable
- 0 Transceiver Disabled (Tri-State)
- 1 Transceiver Enabled

D30 Internal Termination Disabled
- 0 120 Ohm Termination enabled by default (Internal to transceivers) - Default
- 1 Internal Termination disabled – external resistor pack SIPs may be installed

D29 External Loopback Mode

When Cable Transceiver is enabled (Bit D31), this bit will automatically loopback the TxD/RxD, and RTS/CTS signals at the cable (transceivers enabled).
- The DCE/DTE mode will select the set of signals (DCE or DTE) to be looped back
- Since the transceivers will be enabled in this mode, all external cables should be disconnected to prevent interference from external sources.

D28 DTE/DCE Mode (transceiver direction)

See Section 5.3 for a detail of the signal direction as defined for each mode.
- 0 DTE Configuration
- 1 DCE Configuration

D27:24	Xcvr Protocol	0000	RS-422 / RS-485
		All Others	Reserved
D23	Int LB	0	Normal Mode
		1	Internal Loopback –TxD/RXD, RTS/CTS looped back internally
D22:8	RESERVED		
D7:6	GPIOD Src	00	Disabled
		01	Input
		10	0 - Output
		11	1 - Output
D5:4	GPIOC Src	00	Disabled
		01	Input
		10	0 - Output
		11	1 - Output
D3:2	GPIOB Src	00	Disabled
		01	Input
		10	0 - Output
		11	1 - Output
D1:0	GPIOA Src	00	Disabled
		01	Input
		10	0 - Output
		11	1 – Output

2.11 Channel Pin Status: Local Offset 0x0090 / 0x0094 / 0x0098 / 0x009C

In addition to standard inputs, unused inputs may be utilized as general purpose input signals. The Channel Pin Status Register allows the input state of all the IO pins to be monitored. Output signals as well as inputs are included to aid in debug operation.

D31:D8	RESERVED
D7	CTS_DTE Input
D6	CTS_DCE Input
D5	RXD_DTE Input
D4	RXD_DCE Input
D3	GPIOD Input
D2	GPIOC Input
D1	GPIOB Input
D0	GPIOA Input

2.12 Programmable Clock Registers: Local Offset 0x00A0 / 0x00A4 / 0x00A8

The Programmable Clock Registers allow the user to program the on-board programmable oscillator and configure the channel clock post-dividers. As GSC should provide software routines to program the clock, the user should have no need to access these registers. See Section 4.6 for more information.

2.13 Gap Register: Local Offset 0x00B0 / 0x00B4 / 0x00B8 / 0xBC

The Gap Register adds extra Stop bits at the end of the Tx Byte.

D31:D16	Reserved
D15:D0	Additional number of stop bits to insert between transmit bytes

2.14 FIFO Count Register: Local Offset 0x00D0 / 0x00D4 / 0x00D8 / 0x00DC

The FIFO Count Registers display the current number of words in each FIFO. This value, along with the FIFO Size Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs.

D31:D16	Number of words in Rx FIFO
D15:D0	Number of words in Tx FIFO

2.15 FIFO Size Register: Local Offset 0x00E0 / 0x00E4 / 0x00E8 / 0x00EC

The FIFO Size Registers display the sizes of the installed data FIFOs. This value is calculated at power-up. This value, along with the FIFO Count Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs.

D31:D16	Size of installed Rx FIFO
D15:D0	Size of installed Tx FIFO

2.16 Firmware Type Register: Local Offset 0x00F8

This Firmware Type Register shows the FW type of each channel.
All channels are fixed for Fast Async. 08=FASYNC;

D31:D24	Channel 4 FW Type
D23:D16	Channel 3 FW Type
D15:D8	Channel 2 FW Type
D7:D0	Channel 1 FW Type

2.17 Features Revision Register: Local Offset 0x00FC

The Features Revision Register allows software (drivers) to account for added features in the firmware versions. Bits will be assigned as new features are added. See Appendix B for more details.

CHAPTER 3: PROGRAMMING

3.1 Async Serial Interface Definition

The Async Control/Status Registers, Pin Source Registers, and Channel Control Registers contain options to customize the Fast Async serial interface.

The simple fast asynchronous interface consists of two Data signals (TxD /RxD) and two optional Control signals (RTS / CTS). The RTS / CTS handshake signals can be used to pause the transmitter.

The Data Word length is set at 8 Bits and is transmitted LSB first. An optional Even / Odd / Mark / Space Parity bit can be added at the end of the word. Stop Bits can be set to 1 or 2, and further Stop bits can be added using the TxGap register.

3.2 TxGap

The TxGap register defines the number of idle clock cycles between words (Extra Stop Bits). This configurability allows this board to interface with a custom user interface.

3.3 FIFOs

Deep transmit and receive FIFOs are the key to providing four high speed serial channels without losing data. Several features have been implemented to help in managing the on-board FIFOs. These include FIFO flags (Empty, Full, Almost Empty and Almost Full) presented as both real-time status bits and interrupt sources, and individual FIFO counters to determine the exact FIFO fill level. DMA of data to/from the FIFOs provides for fast and efficient data transfers.

A single register is used to access both transmit and receive FIFOs for each channel. Data written to this register will be written to the transmit FIFO, and data read from this register retrieves data from the receive FIFO. Individual resets for the FIFOs are also provided in the Channel Control/Status Register.

3.4 FIFO Flags

Four FIFO flags are present from each on-board FIFO: FIFO Empty, FIFO Full, FIFO Almost Empty, and FIFO Almost Full. These flags may be checked at any time from the Channel Control/Status Register. Note these flags are presented as active low signals (‘0’ signifies condition is true). The Empty and Full flags are asserted when the FIFO is empty or full, respectively. The Almost Empty and Almost Full flags are software programmable such that they may be asserted at any desired fill level. This may be useful in determining when a data transfer is complete or to provide an indicator that the FIFO is in danger of overflowing and needs immediate service.

The Almost Flag value represents the number of bytes from each respective “end” of the FIFO. The Almost Empty value represents the number of bytes from empty, and the Almost Full value represents the number of bytes from full (NOT the number of bytes from empty). For example, the default value of “0x0007 0007” in the FIFO Almost Register means that the Almost Empty Flag will indicate when the FIFO holds 7 bytes or fewer. It will transition as the 8^{th} byte is read or written. In this example, the Almost Full Flag will indicate that the FIFO contains (FIFO Size – 7) bytes or more. For the standard 32Kbyte FIFO, an Almost Full value of 7 will cause the Almost Full flag to be asserted when the FIFO contains 32761 (32k – 7) or more bytes of data.

The values placed in the FIFO Almost Registers take effect immediately, but should be set while the FIFO is empty (or the FIFO should be reset following the change).

3.5 FIFO Counters

Real-time FIFO counters report the exact number of data words currently in each FIFO., allowing the user to determine the exact amount of data which can safely be transferred to the transmit FIFOs or transferred from the receive FIFO. This information should help streamline data transfers by eliminating the need to continuously check empty and full flags, yet still allow larger data blocks to be transferred.

3.6 FIFO Size

The PCIE4-SIO8BX2V-FASYNC provides 32K FIFOs for both the transmitter and receiver for each channel.

3.7 Board vs. Channel Registers

Since four serial channels are implemented on a single board, some registers apply to the entire board, while others are unique to each channel. It is intended that each channel can act independently, but the user must keep in mind that certain accesses will affect the entire board. Typically, the driver will adequately handle keeping board and channel interfaces separate. However, the user must also be mindful that direct access to certain registers will affect the entire board, not just a specific channel.

The Board Control and Board Status registers provide board level controls. Fundamentally, a board reset will do just that, reset all the GSC registers and FIFOs to their default state. Interrupt control is also shared among all registers, although local bits are segregated by channel. The device driver should take care of appropriately handling the inter-mixed channel interrupts and pass them on to the application appropriately.

3.8 Programmable Oscillator / Programmable Clocks

The On-Board Programmable Oscillator provides each channel with a unique programmable clock source using a Cypress Semiconductor CY22393 Programmable Clock generator. In order to program the oscillator, it is necessary to calculate and program values for different clock frequencies. General Standards has developed routines to calculate the necessary values for a given setup and program the clock generator. These clock setup routines have been incorporated into most of the drivers.

The default clock configuration at power-up for the programmable clock on all channels is 20MHz. See Appendix A for more detailed information concerning programming the on-board clock frequencies, as well as common frequency setups. The specific driver manual should have information on clock setup. If not, please contact GSC tech support for assistance.

3.9 Transceiver Protocol Control

The PCIe4-SIO8BX2V-FASYNC is fixed for RS-485 only.

3.10 DCE/DTE Mode

As all signals are bidirectional, the DCE or DTE mode will set the direction for each signal. For the transceivers to be configured as either DTE or DCE, set the DCE/DTE Enable bit in the Pin Source register (D31). The following table gives the input/output configuration for each signal:

Signal	DTE	DCE
TxD	TxD Out	RxD In
RxD	RxD In	TxD Out
RTS	RTS Out	CTS In
CTS	CTS In	RTS Out
GPIOx	Direction controlled by Pin Source Reg	

3.11 Loopback Modes

For normal operation, the Cable Transceiver Enable bit of the Pin Source Register will turn on the cable transceivers, and the DTE/DCE Mode bit will set the transceiver direction. These bits must be set before any data is transmitted over the user interface.

Additionally, there are several ways to loopback data to aid in debug operations. Data may be physically looped back externally by connecting one channel to another. For DB25 cable applications, this simple loopback method will require a gender changer to connect one channel to another. One channel will be set to DTE mode, the other to DCE mode. Data sent from one channel will be received on the other.

An External Loopback mode (External Loopback bit set in the Pin Source Register) is also provided to loop back data on the same channel without requiring any external cabling. In this mode, the DTE/DCE mode will control the location for the transmit signals (TXD, RTS), and the receive signals will use these same signals as the receive inputs. Since signals are transmitted and received through the transceivers, this mode allows the setup to be verified (including signal polarity) without any external connections. Since external signals could interfere with loopback operation, all cables should be disconnected when running in external loopback mode.

An Internal Loopback Mode is also provided which loops back on the same channel internal to the board. This provides a loopback method which does not depend on DTE/DCE mode or signal polarity. This can remove cable

transceiver and signal setup issues to aid in debugging. If the Cable Transceivers are enabled, the transmit data will still appear on the appropriate transmit pins (based on DTE/DCE Mode setting). The Pin Status register will not reflect internally looped back signals, only signals to/from the transceivers.

3.12 General Purpose IO

The Pin Source and Pin Status Registers provide for simple IO control of all the GPIO signals. For outputs, the output value is set using the appropriate field in the Pin Source Register. All inputs can be read via the Pin Status register.

3.13 Interrupts

The PCIe4-SIO8BX2V-FASYNC has many interrupt sources which are passed to the host CPU via the PCI IRQA. Since there is only one physical interrupt source for the board, the interrupts pass through many "levels" to get multiplexed onto this single interrupt. The interrupt originates in the PCI9056 PCI Bridge, which combines the internal PLX interrupt sources (DMA) with the Local on-board interrupt. The single Local Interrupt is made up of the interrupt sources described in Section 2.8. The user should be aware that interrupts must be enabled at each level for an interrupt to occur. For example, if a FIFO interrupt is used, it must be setup and enabled in the GSC Firmware Interrupt Control Register, as well as enabled in the PCI9056. In addition, the interrupt must be acknowledged and/or cleared at each level following the interrupt. The driver will typically take care of setting up and handling the PCI9056 interrupts as well as most local interrupts. The specific driver manual should have more information on how to handle these interrupts.

3.14 PCI DMA

The PCI DMA functionality allows data to be transferred between host memory and the SIO8BX2V onboard FIFOs with the least amount of CPU overhead. The PCI9056 bridge chip handles all PCI DMA functions, and the device driver should handle the details of the DMA transfer. (Note: DMA refers to the transfer of Data from the on-board FIFOs over the PCI bus. This should not be confused with the DMA mode of the USC – transfer of data between the USC and the on-board FIFOs. This On-Board DMA is setup by the driver and should always be enabled.)

There are two PCI DMA modes – Demand Mode DMA and Non-Demand Mode DMA. Demand Mode DMA refers to data being transferred "on demand". For receive, data will be transferred as soon as it is received into the Rx FIFO. For transmit, data will be transferred to the Tx FIFOs if the FIFO is not full. The Demand Mode DMA transfer size may be larger than the actual Tx/Rx FIFOs. Since the amount of data in the FIFOs depends on the amount of data being transferred across the serial channel, timeouts can occur when the requested DMA transfer does not complete. This is usually due to Tx FIFO full or Rx FIFO empty because of a slower serial channel. If a timeout occurs, and there is no way to determine the exact amount of data which was transferred before the DMA was aborted.

Non-Demand Mode DMA does not check the FIFO empty/full flags before or during the data transfer – it simply assumes there is enough available FIFO space to complete the transfer. If the transfer size is larger than the available data, the transfer will complete with invalid results. To avoid this, the driver should calculate and limit the DMA transfer size based on how much Tx FIFO space is unused, or how much data is in the Rx FIFO.

For Non-Demand DMA Max transfer size:

Tx FIFO available space	= Tx FIFO Size (32K) – Tx FIFO Counter
Rx FIFO data available	= Rx FIFO Counter.

CHAPTER 4: PCI INTERFACE

4.0 PCI Interface Registers

The PCI interface is handled by a PCI9056 I/O Accelerator from PLX Technology (Broadcom). The PCI interface is compliant with the 5V, 66MHz 32-bit PCI Specification 2.2. The PCI9056 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 264MB/s to the PCI interface. To reduce CPU overhead during DMA transfers, the controller also implements Chained (Scatter/Gather) DMA, as well as Demand Mode DMA.

Since many features of the PCI9056 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9056 User's Manual. Only those features, which will clarify areas specific to the PCIe4-SIO8BX2V are detailed here. Please refer to the PCI9056 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9056 interface. Unless the user is writing a device driver, the details of this PCI Interface Chapter may be skipped.

4.1 PCI Registers

The PLX 9056 contains many registers, many of which have no effect on the SIO8BX2V performance. The following section attempts to filter the information from the PCI9056 manual to provide the necessary information for a SIO8BX2V specific driver.

The SIO8BX2V uses an on-board serial EEPROM to initialize many of the PCI9056 registers after a PCI Reset. This allows board specific information to be preconfigured correctly.

4.1.1 PCI Configuration Registers

The PCI Configuration Registers allow the PCI controller to identify and control the cards in a system.

PCI device identification is provided by the Vendor ID/Device ID (Addr 0x0000) and Sub-Vendor ID/Sub-Device ID Registers (0x002C). The following definitions are unique to the General Standards SIO8BX2V boards. All drivers should verify the ID/Sub-ID information before attaching to this card. These values are fixed via the Serial EEPROM load following a PCI Reset, and cannot be changed by software.

Vendor ID	0x10B5	PLX Technology
Device ID	0x9056	PCI9056
Sub-Vendor ID	0x10B5	PLX Technology
Sub-Device ID	0x3198	GSC SIO4BXR/SIO8BX2V

The configuration registers also setup the PCI IO and Memory mapping for the SIO8BX2V. The PCI9056 is setup to use PCIBAR0 and PCIBAR1 to map the internal PLX registers into PCI Memory and IO space respectively. PCIBAR2 will map the Local Space Registers into PCI memory space, and PCIBAR3 is unused. Typically, the OS will configure the PCI configuration space.

For further information of the PCI configuration registers, please consult the PLX Technology PCI9056 Manual.

4.1.2 Local Configuration Registers

The Local Configuration registers give information on the Local side implementation. These include the required memory size. The SIO8BX2V memory size is initialized to 4k bytes. All other Local Registers initialize to the default values described in the PCI9056 Manual.

4.1.3 Runtime Registers

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers are not used and serve no purpose on the SIO8BX2V. All other Runtime Registers initialize to the default values described in the PCI9056 Manual.

4.1.4 DMA Registers

The Local DMA registers are used to setup the DMA transfers to and from the on-board FIFOs. DMA is supported only to the four FIFO locations. The SIO8BX2V supports both Demand (DREQ# controlled) and Non-Demand mode DMA. Both Channel 0 and Channel 1 DMA are supported.

4.1.4.1 DMA Channel Mode Register: (PCI 0x80 / 0x94)

The DMA Channel Mode register must be setup to match the hardware implementation.

Bit	Description	Value	Notes
D1:0	Local Bus Width	11 = 32 bit 00 = 8 bit	Although the serial FIFOs only contain 8 bits of data, the register access is still a 32bit access. It is possible to "pack" the data by setting the Local Bus Width to 8, but this is only guaranteed to work with Non-Demand Mode DMA
D5:2	Internal Wait States	0000 = Unused	
D6	Ready Input Enable	1 = Enabled	
D7	Bterm# Input Enabled	0 = Unused	
D8	Local Burst Enable	1 = Supported	Bursting allows fast back-to-back accesses to the FIFOs to speed throughput
D9	Chaining Enable (Scatter Gather DMA)	X	DMA source addr, destination addr, and byte count are loaded from memory in PCI Space.
D10	Done Interrupt Enable	X	DMA Done Interrupt
D11	Local Addressing Mode	1 = No Increment	DMA to/from FIFOs only
D12	Demand Mode Enable	X	Demand Mode DMA is supported for FIFO accesses on the SIO4BXR/SIO8BX2V. (See Section 3.3)
D13	Write & Invalidate Mode	X	
D14	DMA EOT Enable	0 = Unused	
D15	DMA Stop Data Transfer Enable	0 = BLAST terminates DMA	
D16	DMA Clear Count Mode	0 = Unused	
D17	DMA Channel Interrupt Select	X	
D31:18	Reserved	0	

CHAPTER 5: HARDWARE CONFIGURATION

5.0 Board Layout

The following figure is a drawing of the physical components of the PCIe4-SIO8BX2V:

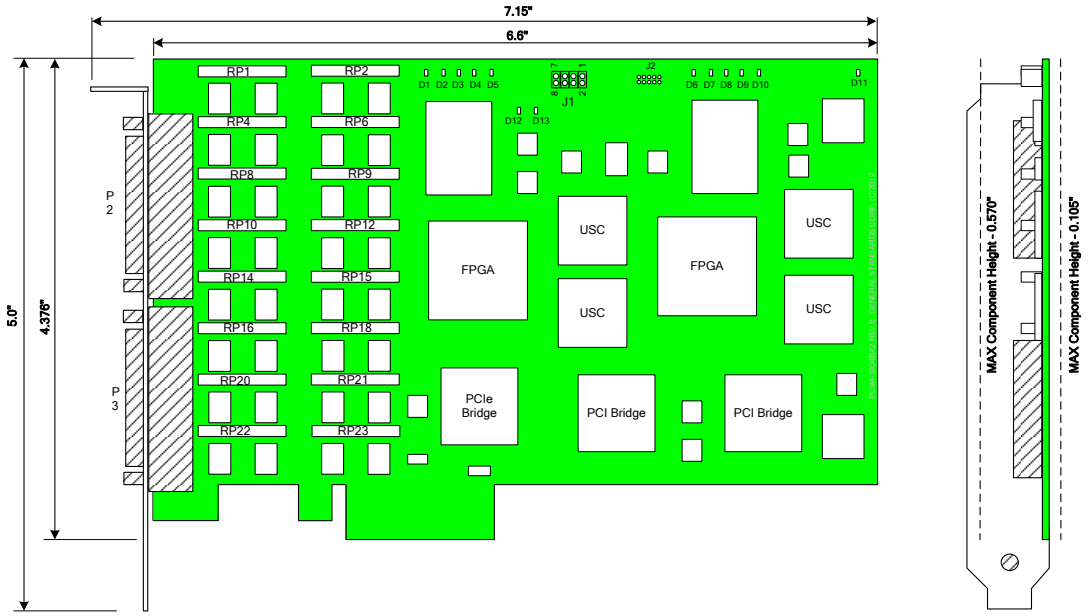


Figure 5-1: Board Layout – Top

5.1 Board ID Jumper J1

Jumper J1 allows the user to set the Board ID in the GSC Board Status Register (See Section 2.1.3). This is useful to uniquely identify a board if more than one SIO8BX2V card is in a system. When the Board ID jumper is installed, it will read '1' in the Board Status Register. The Board Status Register bit will report '0' when the jumper is removed. Refer to Figure 5-1 for Jumper J1 location.

J1 Jumper	Description	Notes
1 - 2	Board ID 1	Board ID 1 in Board Status Register (D0)
3 - 4	Board ID 2	Board ID 2 in Board Status Register (D1)
5 - 6	Board ID 3	Board ID 3 in Board Status Register (D2)
7 - 8	Board ID 4	Board ID 4 in Board Status Register (D3)

5.2 Termination Resistors

The PCIe4-SIO8BX2V board is designed to use either internal 120 Ohm resistors (internal to transceivers) orsocketed external parallel termination (if a different value than the internal termination is required). The external termination resistors are 8 pin SIPs. There are 16 termination SIPs – RP1, RP2, RP4, RP6, RP8, RP9, RP10, RP12, RP14, RP15, RP16, RP18, RP20, RP21, RP22, and RP23. The external parallel resistors are for RS422/RS485 termination only. Refer to Figure 5-1 for resistor pack locations.

Please contact quotes@generalstandards.com if a different termination value is required.

5.3 LEDs

Ten green LEDs (D1-D10) are accessible via software, five to each 4 channel board Refer to Figure 5-2 for these LED locations.

LED D1/D6 is controlled from the Board Control Register. LED D1/D6 Red is controlled by D25, and LED D1/D6 Green is controlled D24.

The remaining 4 LEDs are controlled from D23:D20 of the four Channel Control Registers. Each Channel Control Register controls 1 LED. If D23:D22="10", the Red LED will turn off. Likewise, if D23:D22="11", the Red LED will turn on. D21:D20 controls the Green LED in the pair.

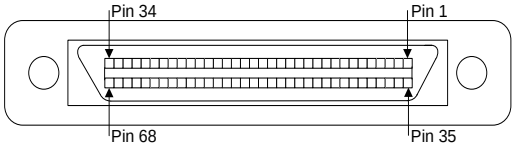
LED_D2/D7 is controlled by Ch 4
LED_D3/D8 is controlled by Ch 3
LED_D4/D9 is controlled by Ch 2
LED_D5/D10 is controlled by Ch 1

Additionally, if all the LED controls are set to 0 in all four of the Channel Control Registers (power up default), the LEDs will display the lower 4 bits of the firmware revision in Green LED_D2/D7 to LED_D5/D10.

The remaining 2 LEDs (D12/D13) display the firmware status. Both LEDs should flash at power up or after a PCIe reset, then will turn off. These LEDs should be off during normal operation.

5.4 Interface Connector

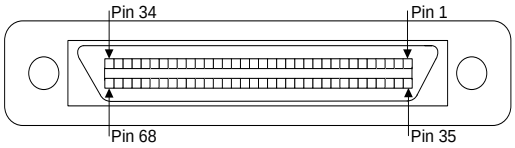
User I/O Connector: 68-pin VHDCI connector (receptacle)
Part Number: TE Connectivity 5796055-1
Mating Connector: TE Connectivity 5787131-3 (or equivalent)



Pin #	RS422/RS485		Pin #	RS422/RS485	
	DTE	DCE		DTE	DCE
1	GPIOD5+		35	GPIOD7+	
2	GPIOD5-		36	GPIOD7-	
3	GPIOC5+		37	GPIOC7+	
4	GPIOC5-		38	GPIOC7-	
5	CTS5+	RTS5+	39	CTS7+	RTS7+
6	CTS5-	RTS5-	40	CTS7-	RTS7-
7	RXD5+	TXD5+	41	RXD7+	TXD7+
8	RXD5-	TXD5-	42	RXD7-	TXD7-
9	GPIOB6+		43	GPIOB7+	
10	GPIOB6-		44	GPIOB7-	
11	RTS5+	CTS5+	45	RTS7+	CTS7+
12	RTS5-	CTS5-	46	RTS7-	CTS7-
13	TXD5+	RXD5+	47	TXD7+	RXD7+
14	TXD5-	RXD5-	48	TXD7-	RXD7-
15	GPIOA5+		49	GPIOA7+	
16	GPIOA5-		50	GPIOA7-	
17	SGND5		51	SGND7	
18	SGND6		52	SGND8	
19	CTS6+	RTS6+	53	CTS8+	RTS8+
20	CTS6-	RTS6-	54	CTS8-	RTS8-
21	RXD6+	TXD6+	55	RXD8+	TXD8+
22	RXD6-	TXD6-	56	RXD8-	TXD8-
23	GPIOA6+		57	GPIOA8+	
24	GPIOA6-		58	GPIOA8-	
25	RTS6+	CTS6+	59	RTS8+	CTS8+
26	RTS6-	CTS6-	60	RTS8-	CTS8-
27	TXD6+	RXD6+	61	TXD8+	RXD8+
28	TXD6-	RXD6 -	62	TXD8-	RXD8-
29	GPIOB6+		63	GPIOB8+	
30	GPIOB6-		64	GPIOB8-	
31	GPIOC6+		65	GPIOC8+	
32	GPIOC6-		66	GPIOC8-	
33	GPIOD6+		67	GPIOD8+	
34	GPIOD6-		68	GPIOD8-	

Table 1- Front Panel (P2) IO Connections

User I/O Connector: 68-pin VHDCI connector (receptacle)
Part Number: TE Connectivity 5796055-1
Mating Connector: TE Connectivity 5787131-3 (or equivalent)



Pin #	RS422/RS485 DTE	RS422/RS485 DCE	Pin #	RS422/RS485 DTE	RS422/RS485 DCE
1	GPIOD1+		35	GPIOD3+	
2	GPIOD1-		36	GPIOD3-	
3	GPIOC1+		37	GPIOC3+	
4	GPIOC1-		38	GPIOC3-	
5	CTS1+	RTS1+	39	CTS3+	RTS3+
6	CTS1-	RTS1-	40	CTS3-	RTS3-
7	RXD1+	TXD1+	41	RXD3+	TXD3+
8	RXD1-	TXD1-	42	RXD3-	TXD3-
9	GPIOB1+		43	GPIOB3+	
10	GPIOB1-		44	GPIOB3-	
11	RTS+	CTS1+	45	RTS3+	CTS3+
12	RTS1-	CTS1-	46	RTS3-	CTS3-
13	TXD1+	RXD1+	47	TXD3+	RXD3+
14	TXD1-	RXD1-	48	TXD3-	RXD3-
15	GPIOA1+		49	GPIOA3+	
16	GPIOA1-		50	GPIOA3-	
17	SGND1		51	SGND3	
18	SGND2		52	SGND4	
19	CTS2+	RTS2+	53	CTS4+	RTS4+
20	CTS2-	RTS2-	54	CTS4-	RTS4-
21	RXD2+	TXD2+	55	RXD4+	TXD4+
22	RXD2-	TXD2-	56	RXD4-	TXD4-
23	GPIOA2+		57	GPIOA4+	
24	GPIOA2-		58	GPIOA4-	
25	RTS2+	CTS2+	59	RTS4+	CTS4+
26	RTS2-	CTS2-	60	RTS4-	CTS4-
27	TXD2+	RXD2+	61	TXD4+	RXD4+
28	TXD2-	RXD2 -	62	TXD4-	RXD4-
29	GPIOB2+		63	GPIOB4+	
30	GPIOB2-		64	GPIOB4-	
31	GPIOC2+		65	GPIOC4+	
32	GPIOC2-		66	GPIOC4-	
33	GPIOD2+		67	GPIOD4+	
34	GPIOD2-		68	GPIOD4-	

Table 2- Front Panel (P3) IO Connections

CHAPTER 6: ORDERING OPTIONS

6.0 Ordering Information

PCIe4 – SIO8BX2V - FASYNC

6.1 Interface Cable

General Standards Corporation can provide an interface cable for the SIO8BX2V board. This standard cable is a twisted pair cable for increased noise immunity. Several standard cable lengths are offered, or the cable length can be custom ordered to the user's needs. Versions of the cable are available with connectors on both ends, or the cable may be ordered with a single connector to allow the user to adapt the other end for a specific application. A standard cable is available which will breakout the serial channels into eight DB25 connectors. Shielded cable options are also available. Please consult our sales department for more information on cabling options and pricing.

6.2 Device Drivers

General Standards has developed many device drivers for the SIO8BX2V boards, including Windows and Linux. As new drivers are always being added, please consult our website (www.generalstandards.com) or consult our sales department for a complete list of available drivers and pricing.

6.3 Custom Applications

Although the SIO8BX2V board provides extensive flexibility to accommodate most user applications, a user application may require modifications to conform to a specialized user interface. General Standards Corporation has worked with many customers to provide customized versions based on the SIO8BX2V boards. Please consult our sales department with your specifications to inquire about a custom application.

APPENDIX A: PROGRAMMABLE OSCILLATOR PROGRAMMING

The 4 on-baord clock frequencies are implemented via two Cypress Semiconductor CY22393 Programmable Clock Generators. In order to change the clock frequencies, this chip must be reprogrammed. This document supplies the information necessary to reprogram the on-board clock frequencies. GSC has developed routines to calculate and program the on-board oscillator for a given set of frequencies, so the user shouuld not need the following information – it is provided for documentation purposes. Contact GSC for help in setting up the on-board oscillator.

The CY22393 contains several internal address which contain the programming information. GSC has mirrored this data internal to the FPGA (CLOCK RAM) to allow the user to simply setup the data in the FPGA RAM and then command the on-board logic to program the clock chip. This isolates the user from the hardware serial interface to the chip. For detailed CY22393 programming details, please refer to the Cypress Semiconductor CY22393 dat sheet.

For the SIO8BX2V, a second programmable oscillator has been added to assure that each channel has a dedicated PLL. (The older SIO4BX uses 3 PLLs in a single CY22393 to generate all four clocks). To implement this, a second CLOCK RAM block was added. CLOCK RAM1 programs the first CY22393 (using CLKA=Ch1_Clk, CLKB=Ch2_Clk, CLKC=Ch3_Clk), and CLOCK_RAM2 programs the second CY22393 (using CLKD=Ch4_Clk). Since the original SIO4BX (with a single CY22393) used CLKD for Ch4_Clk, the same code can be made to support both schemes by simply programming CLKD of the first CY22393.

Each CLOCK RAM block is accessed through 2 registers – Address Offset at local offset 0x00A0 and Data at local offset 0x00A4 (CLOCK RAM1) or 0x00AC (CLOCK RAM2). The user simply sets the RAM Address register to the appropriate offset, then reads or writes the the RAM data. The Programmable Osc Control/Status register allows the user to program the CY22393 or setup the clock post-dividers.

The GSC Local Programmable Clock Registers are defined as follows:

0x00A0 – RAM Address Register

Defines the internal CLOCK RAM address to read/write

0x00A4 – RAM Data1 Register

Provides access to the CLOCK RAM1 pointed to by the RAM Addr Register.

0x00AC – RAM Data2 Register

Provides access to the CLOCK RAM2 pointed to by the RAM Addr Register.

0x00A8 – Programmable Osc Control/Status Register

Provides control to write the contents of the CLOCK RAM to the CY22393 and setup additional post-dividers for the input clocks.

Control Word (Write Only)

D0	Program Oscillator 1 = Program contents of CLOCK RAM to CY22393. Automatically resets to 0.
D1	Measure Channel 1 Clock
D2	Measure Channel 2 Clock
D3	Measure Channel 3 Clock
D4	Measure Channel 4 Clock

D5	Reserved (Unused)
D6	Status Word Readback Control 0 => Status Word D31-D8 == Measured Channel Value 1 => Status Word D31-D8 == Control Word D23-D0
D7	Post-divider set 0 = Ignore D23-D8 during Command Word Write 1 = Set Channel Post-Dividers from D23-D8 during Command Word Write
D11-D8	Channel 1 Post-Divider
D15-D12	Channel 2 Post-Divider
D19-D16	Channel 3 Post-Divider
D23-D20	Channel 4 Post-Divider
D31-D24	Reserved (Unused)

Status Word (Read Only)

D0	Program Oscillator Done 0 = Oscillator Programming in progress.
D1	Program Oscillator Error 1 = Oscillator Programming Error has occurred.
D2	Clock Measurement complete. 0 = Clock Measurement in progress.
D7-D3	Reserved (Unused)
D31-D8	If Command Word D6 = 0, Measured Channel Clock Value If Command Word D6 = 1, Control Word D23-D0

Channel Clock Post-Dividers:

The Control Word defines 4 fields for Channel Clock Post-dividers. These post-dividers will further divide down the input clock from the programmable oscillator to provide for slow baud rates. Each 4 bit field will allow a post divider of 2^n. For example, if the post-divider value=0, the input clock is not post-divided. A value of 2 will provide a post-divide of 4 (2^2). This will allow for a post-divide value of up to 32768 (2^15) for each input clock. Bit D7 of the Control word qualifies writes to the post-divide registers. This allows other bits in the command register to be set while the post-divide values are maintained.

Channel Clock Measurement:

The Control Word defines 4 bits which will select one of the 4 channel clocks (input clock + post-divide) for a measurement. This will allow the user feedback as to whether the programmable oscillator was programmed correctly. To measure a clock, select the clock to measure in the Control word, and also clear Bit D6 to allow for readback of the result. Read back the Status Word until D2 is set. Status Word D31-D8 should contain a value representing 1/10 the measured clock frequency (Value * 10 = Measured Frequency in MHz). Keep in mind that this value will not be exactly the programmed frequency due to the 100ppm (0.01%) accuracy of the on-board reference.

The Internal RAM is defined as follows: RAM Address 0x08–0x57 correspond directly to the CY22393 registers.

Address	Description	Default Value
0x00 – 0x05	Reserved (Unused)	0x00
0x06	Reserved	0xD2
0x07	Reserved	0x08
0x08	ClkA Divisor (Setup0)	0x01
0x09	ClkA Divisor (Setup1)	0x01
0x0A	ClkB Divisor (Setup0)	0x01
0x0B	ClkB Divisor (Setup1)	0x01
0x0C	ClkC Divisor	0x01
0x0D	ClkD Divisor	0x01
0x0E	Source Select	0x00
0x0F	Bank Select	0x50
0x10	Drive Setting	0x55
0x11	PLL2 Q	0x00
0x12	PLL2 P Lo	0x00
0x13	PLL2 Enable/PLL2 P Hi	0x00
0x14	PLL3 Q	0x00
0x15	PLL3 P Lo	0x00
0x16	PLL3 Enable/PLL3 P Hi	0x00
0x17	OSC Setting	0x00
0x18	Reserved	0x00
0x19	Reserved	0x00
0x1A	Reserved	0xE9
0x1B	Reserved	0x08
0x1C-0x3F	Reserved (Unused)	0x00
0x40	PLL1 Q (Setup0)	0x00
0x41	PLL1 P Lo 0 (Setup0)	0x00
0x42	PLL1 Enable/PLL1 P Hi (Setup0)	0x00
0x43	PLL1 Q (Setup1)	0x00
0x44	PLL1 P Lo 0 (Setup1)	0x00
0x45	PLL1 Enable/PLL1 P Hi (Setup1)	0x00
0x46	PLL1 Q (Setup2)	0x00
0x47	PLL1 P Lo 0 (Setup2)	0x00
0x48	PLL1 Enable/PLL1 P Hi (Setup2)	0x00
0x49	PLL1 Q (Setup3)	0x00
0x4A	PLL1 P Lo 0 (Setup3)	0x00
0x4B	PLL1 Enable/PLL1 P Hi (Setup3)	0x00
0x4C	PLL1 Q (Setup4)	0x00
0x4D	PLL1 P Lo 0 (Setup4)	0x00
0x4E	PLL1 Enable/PLL1 P Hi (Setup4)	0x00
0x4F	PLL1 Q (Setup5)	0x00
0x50	PLL1 P Lo 0 (Setup5)	0x00
0x51	PLL1 Enable/PLL1 P Hi (Setup5)	0x00
0x52	PLL1 Q (Setup6)	0x00
0x53	PLL1 P Lo 0 (Setup6)	0x00
0x54	PLL1 Enable/PLL1 P Hi (Setup6)	0x00
0x55	PLL1 Q (Setup7)	0x00
0x56	PLL1 P Lo 0 (Setup7)	0x00
0x57	PLL1 Enable/PLL1 P Hi (Setup7)	0x00
0x58-0xFF	Reserved (Unused)	0x00

APPENDIX B: FIRMWARE REVISIONS / FEATURES REGISTER

Since SIO4 boards can exist across multiple form factors and with various hardware features, the firmware/features registers attempt to help identify the exact version of a SIO4 board. This appendix provides a more detailed breakdown of what the firmware and features registers, and detail differences between the firmware revisions.

Firmware Register - Local Offset 0x00 (0xE508010C)

D31:16 HW Board Rev 0xE508 PCIe4-SIO8BX2V Rev NR/A

- D31 **1** = Features Register Present
- D30 **1** = Complies with this standard
- D29 **1** = 66MHz PCI bus interface
  0 = 33MHz PCI bus interface
- D28 1 = 64 bit PCI bus interface
  0 = 32 bit bus interface
- D27:D24 Form Factor
  0 = Reserved
  1 = PCI
  2 = PMC
  3 = cPCI
  4 = PC104P
  5 = PCIe
  6 = XMC
- D23:D20 HW Board (sub-field of form factor)
  0 = PCIe4-SIO8BX2 / PCIe4-SIO8BX2V
  1 = PCIe-SIO4BX
- D19: HW Board Sub Rev
  0 = PCIe4-SIO8BX2
  1 = PCIe4-SIO8BX2V
- D18:D16 HW Board Rev (lowest rev for firmware version)
  0=NR
  1=A,
  2=B

D15:8 Firmware Type ID

0x01 - Std Firmware
0x04 - Sync Firmware
0x08 – FAsync Firmware (default)

D7:0 Firmware Revision XX Firmware Version

0x00 – Original Release

Feature Register - Local Offset 0xFC (0x00613AF4)

D31:D27	**00000**	Unused
D26	**0**	No Rx Packet FIFO
D25	**0**	No Tx Packet FIFO
D24	**0**	No ~RxC Source
D23	**0**	No Sync Timestamp / Sync Rx Bit Size / Front Panel Timestamp
D22	**1**	Rx Stop on Full
D21	**1**	Test Feature
D20	**0**	No Rx Status byte inserted in FIFO
D19:D18	Timestamp	
	00	not supported
	01	single external clock
	10	single internal clock
D17:D16	FPGA Reprogram field	
	00	Not Present
	01	Present
D15:D14	Configurable FIFO space	
	00	Not Supported
	01	Rx/Tx select. Up to 32k deep FIFOs
D13	**1**	FIFO Test Bit
D12	**1**	FW Type Reg
D11:D8	FW Feature Level (Set at common code level)	
	0x01	RS232 support, Pin Source Change
	0x02	Multi-Protocol support
	0x03	Common Internal/External FIFO Support
	0x04	FIFO Latched Underrun/Overrun/Level
	0x05	Demand mode DMA Single Cycle for Tx
	0x06	DMA_Single_Cycle_Dis, updated Pin_Src
	0x07	Rx Underrun Only, Reset Status
	0x08	Clock to 50Hz with 10Hz resolution
	0x09	No Legacy Support (No Clock Control Register)
	0x0A	Falling Int fix
D7	**1**	DMA Single Cycle Disable
D6	**1**	Board Reset, FIFO present bits
D5	**1**	FIFO Size/Counters present
D4	**1**	FW ID complies with this standard
D3:D0	Clock Oscillator	
	0x0	Fixed
	0x1	ICD2053B (1 Osc)
	0x2	ICD2053B (4 Osc)
	0x3	CY22393 (4 Osc)
	0x4	2 x CY22393 (6 Osc)