

PMC-LVDS CLOCK DRIVER



FEATURES:

- 12 Output Channels (see description below)
- Hardware Sync and Clock I/O for Multiboard Synchronization
- Clock or Sync inputs can be LVDS or TTL.
- Additional LVDS to TTL and TTL to LVDS converters for independent signal conversions (AUX)
- Only +5VDC Required from PCI bus.
- Conforms to PCI Bus Specification, Revision 2.3
- Available on Adapters for Alternate Form Factors: PCI, cPCI, PC104-Plus

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Overview:

The 12-channel PMC-LVDS Clock Driver Board provides a means of distributing LVDS signals among multiple boards, all from within a standard single-width PMC module. Optimized for flexibility and performance, the board is ideal for multi-board synchronization, LVDS to TTL conversion or TTL to LVDS.

Functional Description:

The Board provides two channel groups, A or B, consisting of five LVDS output channels. Each group has an optional input that can be either LVDS or TTL. The selection is made possible via a jumper (J1) residing on the board. The installation of a jumper will assign Group A or B (or both), for LVDS inputs. Removing the jumper will configure the inputs for TTL. Having this option allows one group's input source (Group A) to be configured differently from the other group (Group B). Also, two auxiliary converters (AUX) have been added for independent signal conversion. AUX00 provides a TTL to LVDS conversion. AUX01 provides a LVDS to TTL conversion.

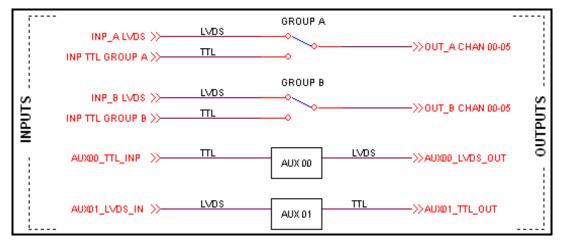


Figure 1. PMC-LVDS Clock Driver; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel through a high-density 68-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification.

ELECTRICAL SPECIFICATIONS

At +25 $^{\rm O}$ C, with specified operating conditions.

Power Requirements:

+5.0 VDC ± 0.25 VDC at 0.75 watts typical. 1.7 watts maximum.

Mechanical Characteristics:

(HxWxD): 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 149.0 mm (5.87 in)(Mechanical dimensions are shown for the native PMC form factor. See Ordering Information.)

Environmental Specifications:

Ambient Temperature Range:`	Operating: Standard: 0 to +65 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius.
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

Ordering Information:

Basic Model Number	Form Factor	
PMC-LVDS Clock Driver	PMC (Native)	
PCI- LVDS Clock Driver *	PCI, short length	
cPCI- LVDS Clock Driver *	cPCI, 3U	

* PMC module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

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SYSTEM I/O CONNECTIONS

I/O CONNECTOR PIN ASSIGNMENTS

PIN FUNCTION 1 GND 2 GND 3 OUT_A CHAN 00 LO 4 OUT_A CHAN 00 LO 4 OUT_A CHAN 00 HI 5 GND 6 GND 7 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LI 9 GND 10 GND 11 OUT_A CHAN 04 LO 12 OUT_A CHAN 04 LO 11 OUT_A CHAN 04 LO 11 OUT_A CHAN 04 LO 12 OUT_A CHAN 04 LO 13 GND 14 GND 15 OUT_B CHAN 00 LO 16 OUT_B CHAN 02 LO 20 OUT_B CHAN 02 LI 21 GND 22 GND 23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 LO 25 GND 26 GND 27 INP AUX01 LO 28	ROW-A		ROW-B		
1 GND 2 GND 3 OUT_A CHAN 00 LO 3 OUT_A CHAN 00 LO 4 OUT_A CHAN 00 HI 5 GND 6 GND 7 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 9 GND 10 GND 11 OUT_A CHAN 04 LO 12 OUT_A CHAN 04 LO 11 INP_A LVDS LO 12 OUT_A CHAN 04 HI 13 GND 14 GND 15 OUT_B CHAN 00 LO 16 OUT_B CHAN 00 LO 16 OUT_B CHAN 02 LO 20 OUT_B CHAN 02 LO 20 OUT_B CHAN 02 LO 21 GND 22 GND 23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 LO 25 GND 26 GND 27 INP AUX01 LO 28 INP AUX01 LO <			· · · · · ·		
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3 OUT_A CHAN 00 LO 4 OUT_A CHAN 00 HI 5 GND 6 GND 7 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 8 OUT_A CHAN 02 LO 9 GND 10 GND 11 OUT_A CHAN 04 LO 12 OUT_A CHAN 04 LO 13 GND 14 GND 15 OUT_B CHAN 04 LO 15 OUT_B CHAN 00 LO 16 OUT_B CHAN 00 LO 16 OUT_B CHAN 02 LO 17 GND 18 GND 19 OUT_B CHAN 02 LO 20 OUT_B CHAN 02 LO 21 GND 22 GND 23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 LO 25 GND 26 GND 27 INP AUX01 LO 28 INP AUX01 HI 29 GND 30 <t< td=""><td></td><td></td><td></td><td></td></t<>					
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17 GND 18 GND 19 OUT_B CHAN 02 LO 20 OUT_B CHAN 02 HI 21 GND 22 GND 23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 HI 25 GND 26 GND 27 INP AUX01 LO 28 INP AUX01 HI 29 GND 30 GND 30 GND 31 OUT AUX00 LO 32 OUT AUX00 HI 33 NC	15	OUT_B CHAN 00 LO	15	OUT_B CHAN 01 LO	
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21 GND 21 GND 22 GND 22 GND 23 OUT_B CHAN 04 LO 23 INP_B LVDS LO 24 OUT_B CHAN 04 HI 24 INP_B LVDS HI 25 GND 26 GND 27 INP AUX01 LO 27 GND 28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 30 OUT AUX00 LO 31 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	19	OUT_B CHAN 02 LO	19	OUT_B CHAN 03 LO	
22 GND 23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 HI 25 GND 26 GND 27 INP AUX01 LO 28 INP AUX01 HI 29 GND 30 GND 31 OUT AUX00 HI 32 OUT AUX00 HI 33 NC	20	OUT_B CHAN 02 HI	20	OUT_B CHAN 03 HI	
23 OUT_B CHAN 04 LO 24 OUT_B CHAN 04 HI 25 GND 26 GND 27 INP AUX01 LO 28 INP AUX01 HI 29 GND 30 GND 31 OUT AUX00 HI 32 OUT AUX00 HI 33 NC	21	GND	21	GND	
24 OUT_B CHAN 04 HI 24 INP_B LVDS HI 25 GND 25 GND 26 GND 26 GND 27 INP AUX01 LO 27 GND 28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 30 OUT AUX00 LO 31 OUT AUX00 LO 31 GND 32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	22	GND	22	GND	
25 GND 25 GND 26 GND 26 GND 27 INP AUX01 LO 27 GND 28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 30 OUT AUX00 LO 30 GND 30 OUT AUX00 LO 32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	23	OUT_B CHAN 04 LO	23	INP_B LVDS LO	
26 GND 26 GND 27 INP AUX01 LO 27 GND 28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 29 GND 30 GND 30 OUT AUX00 LO 31 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	24	OUT_B CHAN 04 HI	24	INP_B LVDS HI	
27 INP AUX01 LO 27 GND 28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 30 OUT AUX00 LO 30 OUT AUX00 HI 31 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	25	GND	25	GND	
28 INP AUX01 HI 28 INP AUX00 TTL 29 GND 29 GND 30 GND 30 OUT AUX00 LO 31 GND 31 OUT AUX00 LO 31 GND 32 INP TTL GROUP A 33 NC 33 GND 33 GND	26	GND	26	GND	
29 GND 29 GND 30 GND 30 OUT AUX01 TTL 31 OUT AUX00 LO 31 GND 32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	27	INP AUX01 LO	27	GND	
30 GND 30 OUT AUX01 TTL 31 OUT AUX00 LO 31 GND 32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	28	INP AUX01 HI	28	INP AUX00 TTL	
31 OUT AUX00 LO 31 GND 32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	29	GND	29	GND	
32 OUT AUX00 HI 32 INP TTL GROUP A 33 NC 33 GND	30	GND	30	OUT AUX01 TTL	
33 NC 33 GND	31	OUT AUX00 LO	31	GND	
	32	OUT AUX00 HI	32	INP TTL GROUP A	
	33	NC	33	GND	
34 INF TIL GROUP B	34	NC	34	INP TTL GROUP B	

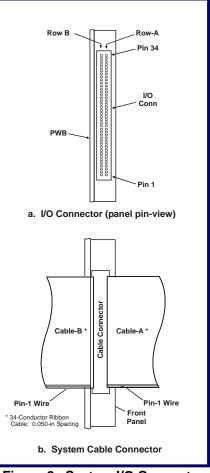


Figure 2. System I/O Connector

System Cable Mating Connector:

68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref): Amp # 787170-7

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8302A Whitesburg Drive · Huntsville, AL 35802 Phone: (256) 880-8787 or (800) 653-9970 FAX: (256) 880-8788 Email: Solutions@GeneralStandards.com