24DSI6LN

24-bit, 6 channel, 200KS/S/Ch Delta-Sigma A/D Input

PC104P-24DSI6LN

Application Note
Improving Sample Rate Accuracy

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Preface

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1. Introduction

This application note is intended to provide a procedure for improving a board's sample rate accuracy.

1.1. Applicability

This document uses a General Standards 24DSI6LN as the centerpiece of a simple procedure for improving sample rate accuracy. The procedure however, can be applied to any board where the master clock, or a fixed derivative of the master clock, can be routed to the board's cable interface.

1.2. Brief Description

The gist of the procedure is to measure the frequency of the board's master clock with high precision, then use that value in the formulas used to calculate the desired sample rate.

1.3. Limitations

The specification for the 24DSI6LN master clock states that the oscillator is stable to within ±25 PPM and that the aging drift is within ±5 PPM per year. The specification provides no information on the oscillator drift over short periods of time, such as minutes, hours, days, weeks or months. The benefit of applying the procedure described herein may therefore be limited. Additionally, in many cases knowing the exact master clock frequency may provide no benefit over using the default frequency.

1.4. Equipment

The following table lists the equipment used by General Standards to measure the frequency of the master clock on a 24DSI6LN. A Linux based host is required for running the software used in this effort.

Item	Description
	One PC104P-24DSI6LN board was used. Any board supported by the 24DSI Linux driver will suffice. The specific model number is not critical. However, a 24DSI32 board will require a different test fixture and corresponding cable.
	The 24DSI12 test fixture is used for signal routing. It routes the `Ext Clk Out` signal from the cable to the corresponding board jumpers. The test fixture is used merely for its convenience. This model test fixture is used with both 24DSI12 and 24DSI6 based model boards. The 24DSI32 model boards require a different test fixture.
	One 24DSI12 cable with 68-pin SCSI connectors on each end. The cable is used for its convenience in connecting the board to the test fixture. This same cable is used with both 24DSI12 and 24DSI6 based model boards. The 24DSI32 model boards require a different cable.
	A high precision counter is used to measure the frequency of the master clock when routed to the `Ext Clk Out` signal at the cable interface.

	An Oscilloscope is used to visually observe and measure the frequency of the master clock when routed to the `Ext Clk Out` signal at the cable interface.
	RG58 cabling is used to feed the `Ext Clk Out` signal to the oscilloscope and the frequency counter.
	Test leads are used to attach the cabling to the `Ext Clk Out` test fixture jumpers.

2. Basic Procedure

This section provides the basics for measuring the frequency of the master clock at the 24DSI6LN cable interface and making use of the measurement.

2.1. Setup

The illustration below depicts how the equipment is connected for measuring the frequency of the 24DSI6LN master clock. A ribbon cable connects the 24DSI6LN to the "Board 2" test fixture connecter. (With the BNC connectors facing away from you, position two is at the left.) The test leads are connected to the Ext Clk Out Lo and Ext Clk Out Hi test points on the central jumper block (black to *low* and red to *high*). The RG58 cables connect the test leads to the oscilloscope and the TTL inputs of the frequency counter.
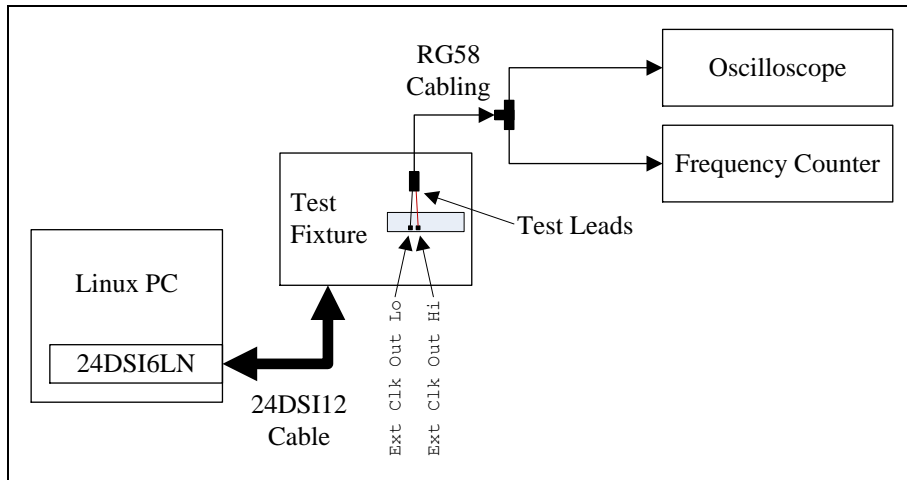

Figure 1 The basic setup for measuring the master clock frequency.

2.2. Making the Measurement

> **NOTE:** Whether in the lab or the field, the environment for all equipment must be stable before taking measurements. If any aspect of the environment has not stabilized, then the results could be unreliable or worse than using the default master clock frequency.

With the equipment powered up and the Linux PC booted, make sure the 24DSI Linux driver is completely installed, built and running. (Refer to the *24DSI Linux Driver User Manual* for instructions.) For the best results wait at least 15 minutes for the system temperature to completely stabilize. Execute the `fref` sample application (…/24dsi/samples/fref) adding the -s# argument with a value for several minutes or more to allow time for observations (i.e. -s600 for 10 minutes). Invoke the oscilloscope's "auto" feature to adjust the capture settings for the input signal. With the frequency measurement feature selected the frequency reported should be approximately 32.768 MHz. The frequency counter, with minor setting adjustments, should also report a frequency that is approximately 32.768 MHz. With the display set to continually update, several of the lower digits will constantly change. This is expected. To stabilize the reading enable the device's averaging feature. Well after the reading has stabilized, record the reading for use in calculating the desired sample rate.

2.3. Using the Measurement

The 24DSI6LN reference manual provides formulas for configuring the on-board resources to produce virtually any valid sample rate. If one uses only the Rate A Generator, then the formulas are effectively as follows.

$$Fsamp = Fref \times \frac{Nvco}{Nref} \times \frac{1}{512 \times DIVISOR}$$

$$DIVISOR = Ndiv \,? \, 0.5 : Ndiv$$

The result, *Fsamp*, is the resulting sample rate while *Nvco*, *Nref* and *Ndiv* are register fields configured to produce that sample rate. In the equation *Fref* is the Frequency of the reference oscillator, which is the master clock. The default frequency is 32.768 MHz and is stable to within ±25 PPM. Any variation in the master clock appears as corresponding variations in the sample rate.

The 24DSI Linux driver incudes a sample application named *fsamp*. The application is designed to evaluate the above formulas and report the configuration that produces the sample rate closest to a requested rate. This application is used in the below examples, in which the value of *Fref* varies over its entire ±25PPM range for selected sample rates. The graphs show the results of the calculations using both the default oscillator frequency and the specified (or presumed known) frequency. The graphs reveal that knowing the oscillator's exact frequency may provide no benefit at all, it may provide a limited benefit or it may provide a definite benefit.

The *fsamp* application can be used to derive the best configuration for all integral sample rates from the minimum of 2,000 S/S to the maximum of 200,000 S/S (when using only a single rate generator). If this is done and the accuracy of the results graphed, it is revealed that, computationally, the board's PLL and other on-board resources produce extremely accurate results. This is depicted in Figure 2. In many cases the desired sample rate can be computed exactly. In the worst case, the results will be within 0.05% of the desired sample rate.

Figure 2 The Fsamp accuracy as produced by the board's PLL and other on-board resources.

2.4. Real World Examples

The figures that follow illustrate the results of knowing the exact master clock frequency and using the previously given formulas with the default frequency and the known frequency. They depict the results of the master clock frequency varying over its entire ±25 PPM range for selected sample rates. The selected sample rates are among those known to be used by our customers.

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2.4.1. Example 1: Fsamp = 8,192 S/S

Computationally, the sample rate of 8,192 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency can help in achieving a more accurate sample rate.
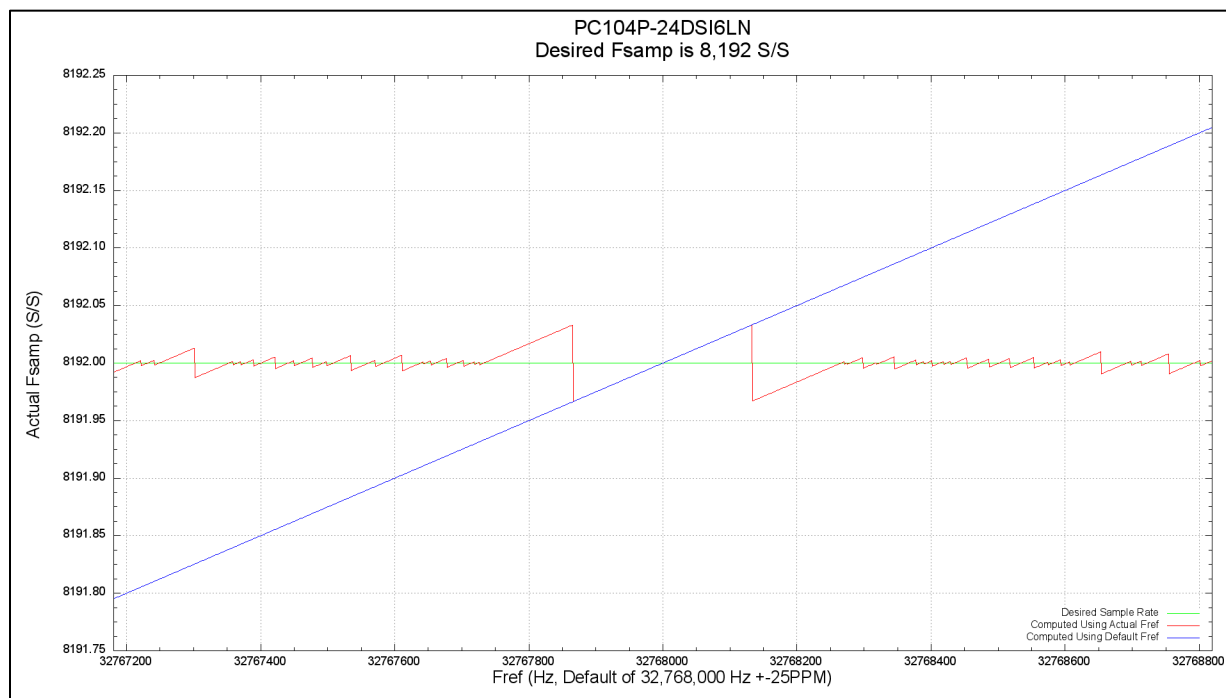

Figure 3 Using the default and known Fref for an Fsamp of 8,192 S/S.

2.4.2. Example 2: Fsamp = 10,000 S/S

Computationally, the sample rate of 10,000 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency may help in achieving a marginally more accurate sample rate.
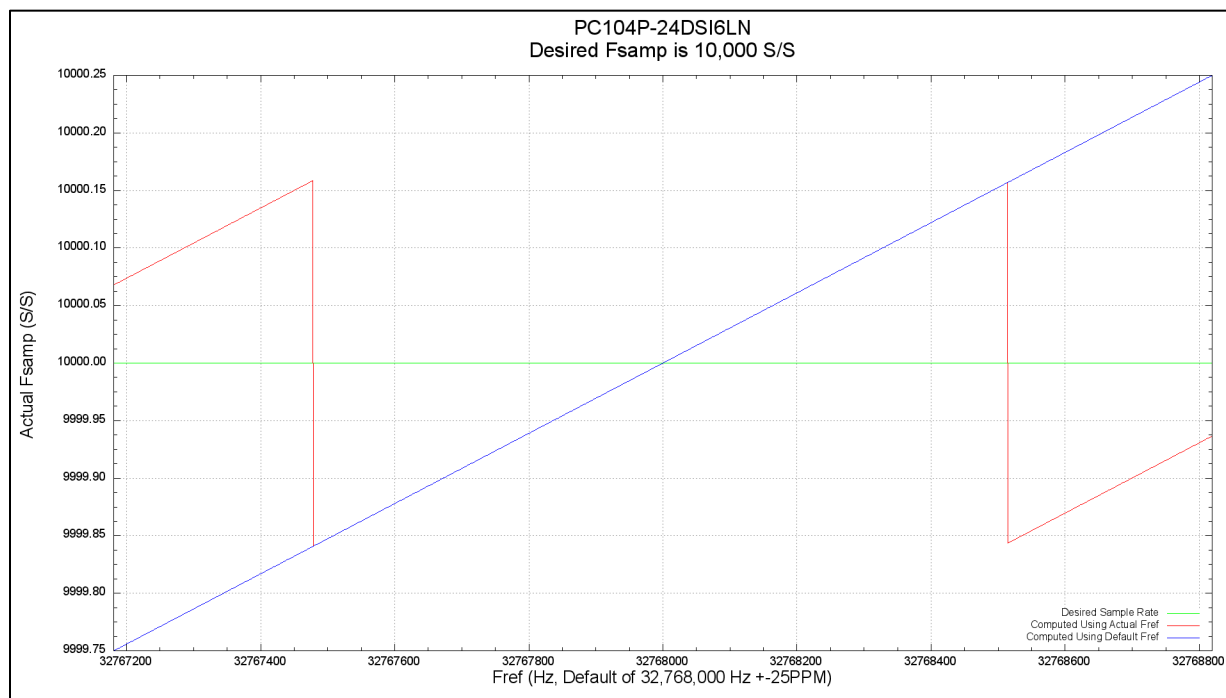

Figure 4 Using the default and known Fref for an Fsamp of 10,000 S/S.

2.4.3. Example 3: Fsamp = 24,000 S/S

Computationally, the sample rate of 24,000 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would not help to achieve a more accurate sample rate. (The red graph is totally concealed behind the blue graph.)

Figure 5 Using the default and known Fref for an Fsamp of 24,000 S/S.

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2.4.4. Example 4: Fsamp = 36,000 S/S

Computationally, the sample rate of 36,000 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would not help to achieve a more accurate sample rate. (The red graph is totally concealed behind the blue graph.)
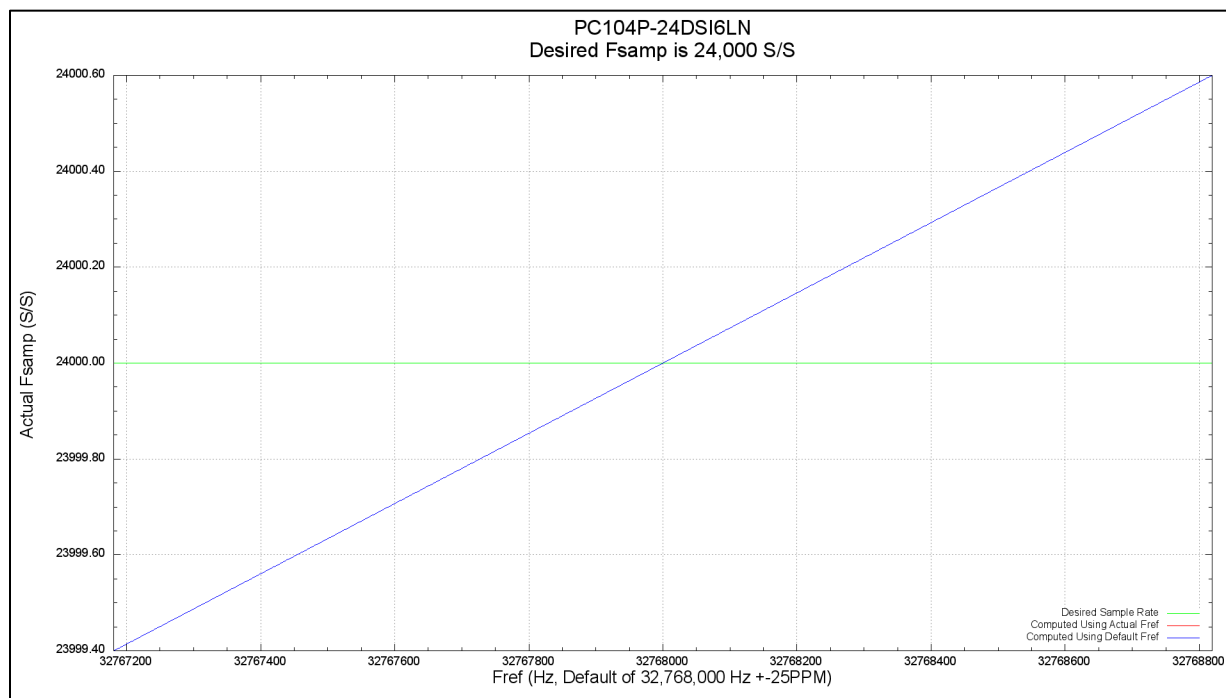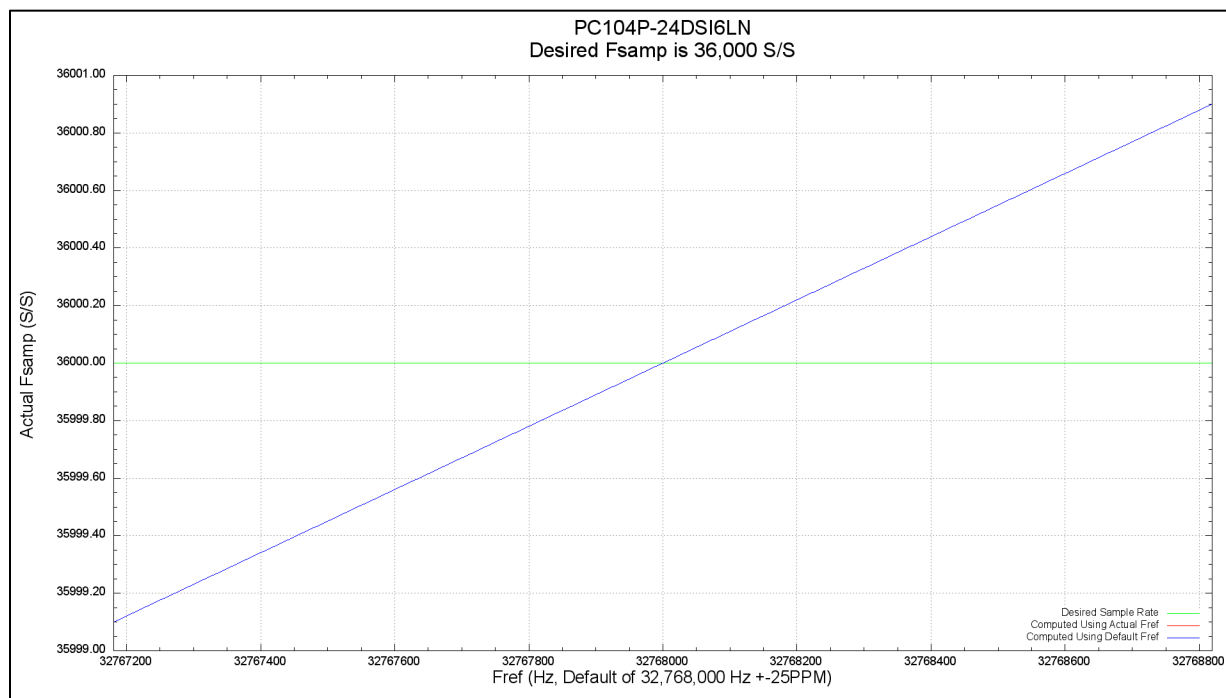

Figure 6 Using the default and known Fref for an Fsamp of 36,000 S/S.

2.5. Alternate Examples

The figures that follow illustrate the results of knowing the exact master clock frequency and using the previously given formulas with the default frequency and the known frequency. They depict the results of the master clock frequency varying over its entire ±25 PPM range for selected sample rates. The sample rates chosen are those which were not expected to produce ideal results.

2.5.1. Example 5: Fsamp = 15,998 S/S

Computationally, the sample rate of 15,998 S/S is among those that cannot be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would help to achieve a marginally more accurate sample rate. (The red graph is partially concealed behind the blue graph.)
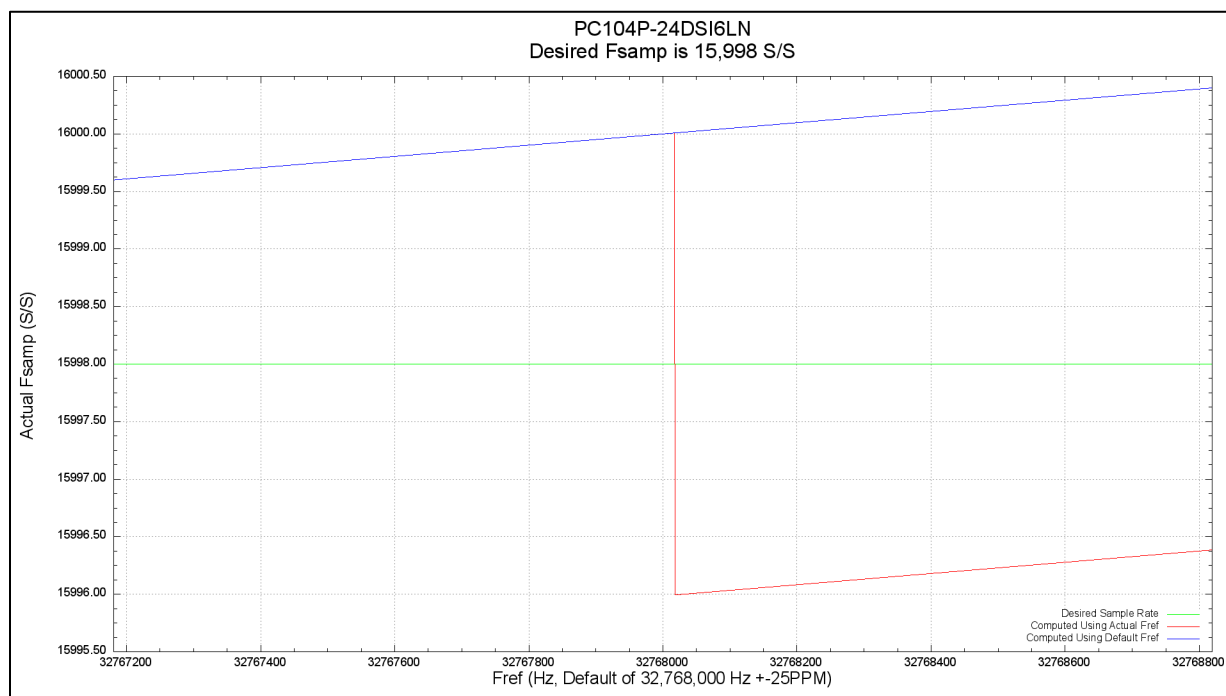

Figure 7 Using the default and known Fref for an Fsamp of 15,998 S/S.

2.5.2. Example 6: Fsamp = 16,020 S/S

Computationally, the sample rate of 16,020 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would help to achieve a more accurate sample rate.
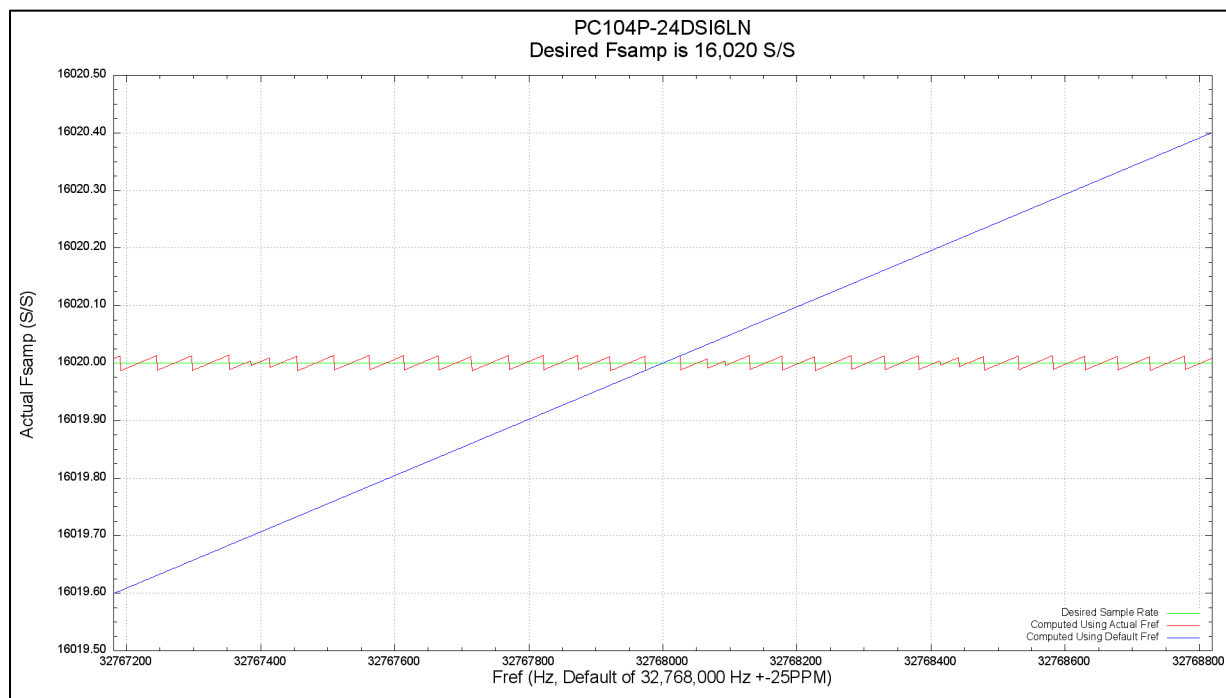

Figure 8 Using the default and known Fref for an Fsamp of 16,020 S/S.

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2.5.3. Example 7: Fsamp = 128,066 S/S

Computationally, the sample rate of 128,066 S/S is among those that cannot be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would help to achieve a marginally more accurate sample rate.
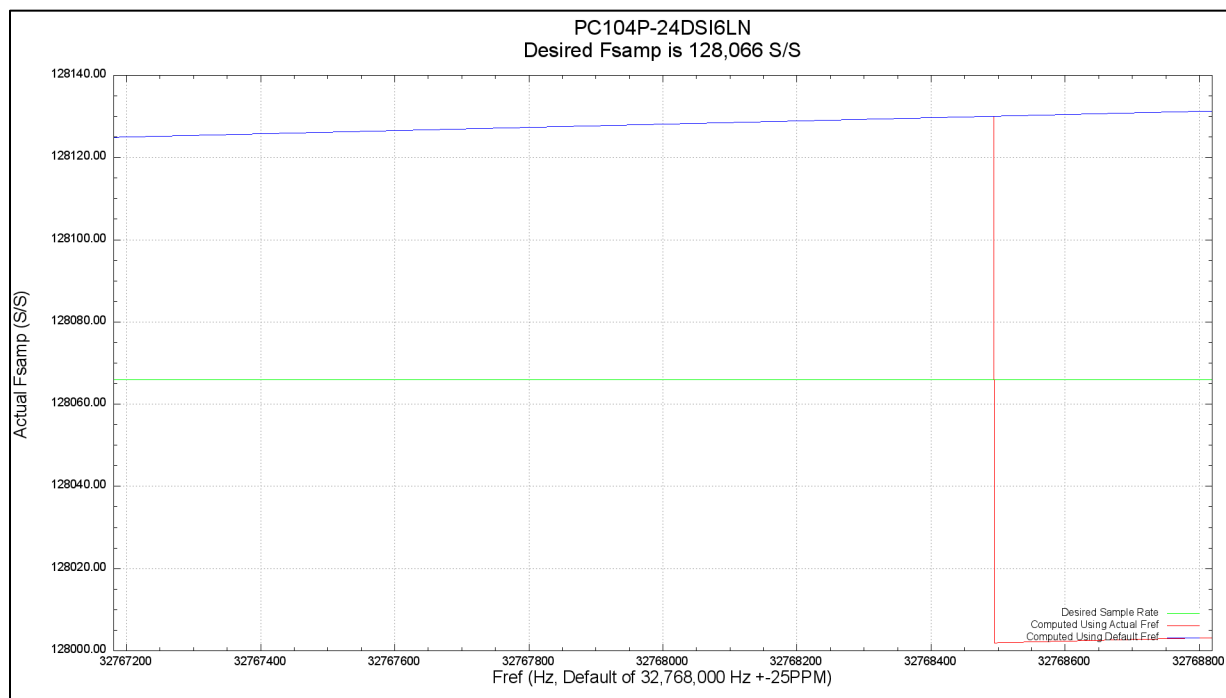

Figure 9 Using the default and known Fref for an Fsamp of 128,066 S/S.

2.5.4. Example 8: Fsamp = 190,000 S/S

Computationally, the sample rate of 190,000 S/S is among those that can be achieved exactly. The achieved rate however, will still vary per the master clock's ±25PPM stability. In this case, knowing the exact oscillator frequency would help to achieve a more accurate sample rate.
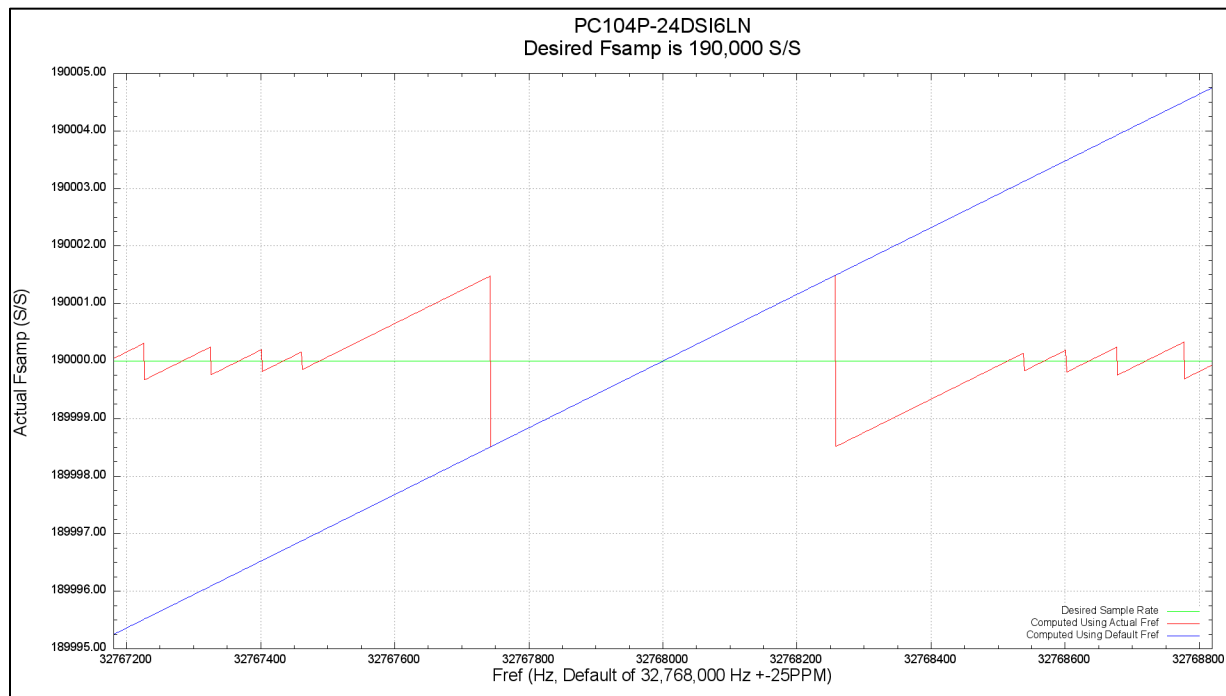

Figure 10 Using the default and known Fref for an Fsamp of 190,000 S/S.

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3. Test Fixture

The test fixture is available from General Standards. The following are the available diagrams.
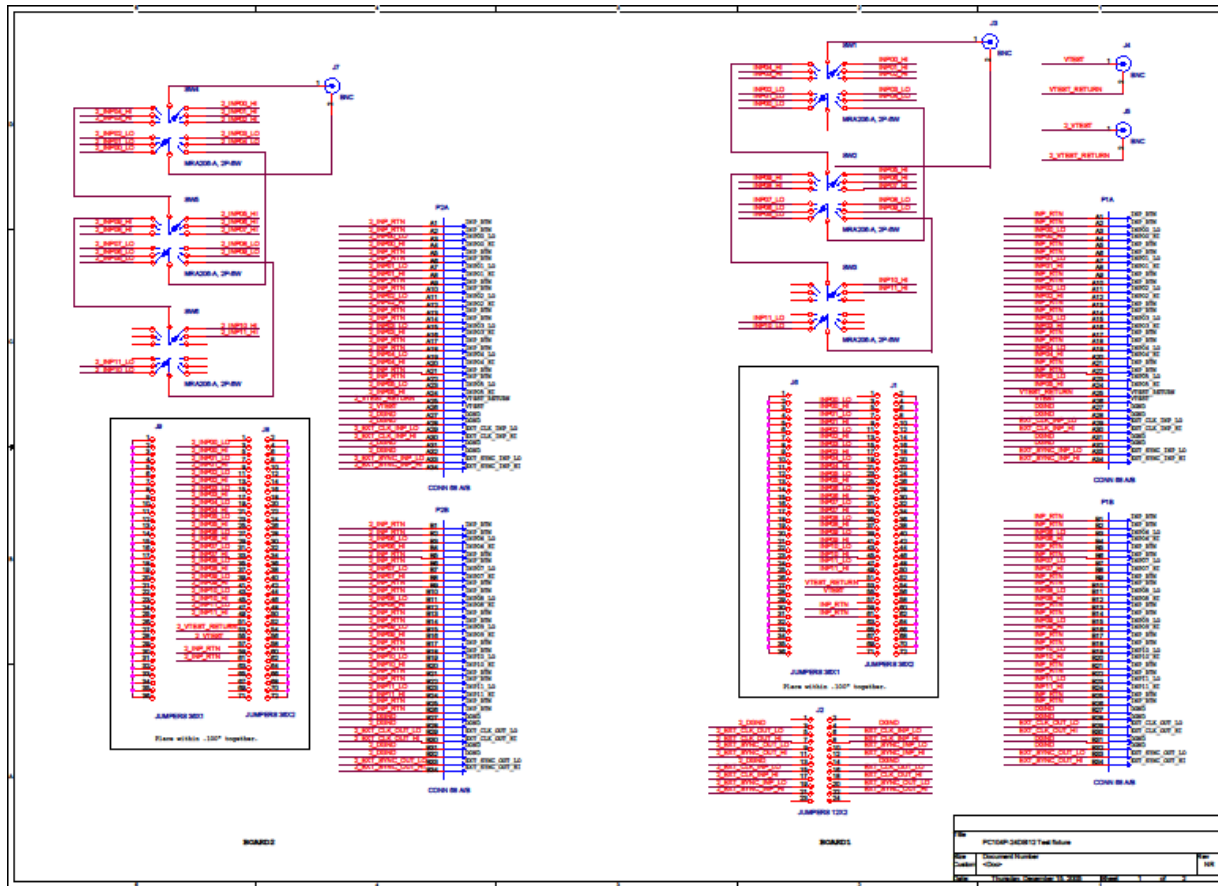

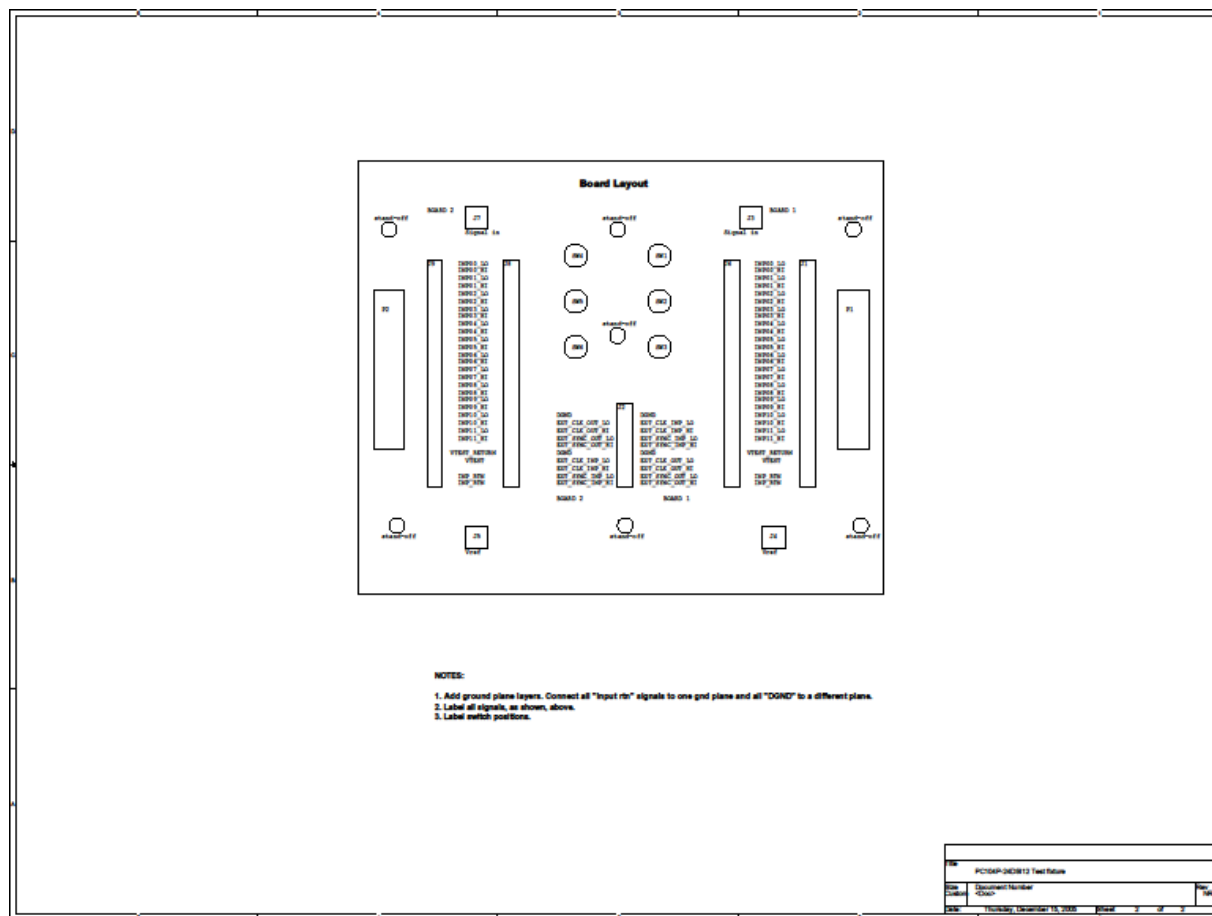**Figure 11** A schematic of the 24DSI12 test fixture.

Figure 12 A diagram of the 24DSI12 test fixture.

Document History

Revision	Description
November 21, 2022	Minor editorial updates.
April 25, 2022	Updated the release date.
April 25, 2019	Updated the release date.
April 22, 2019	Updated the release date.
November 5, 2018	Updated the inside cover page.
December 26, 2017	This is the initial release.